PRINCIPLES OF OPERATION

INTRODUCTION

Principles of operation describes Monitor principles of operation, beginning with functional block diagram descriptions. This is followed by detailed component descriptions of each of the major Monitor subassemblies. Schematic diagrams are linked to throughout. Also included, a description of the general principles of operation of the interchangeable modules.

FUNCTIONAL PRINCIPLES OF OPERATION

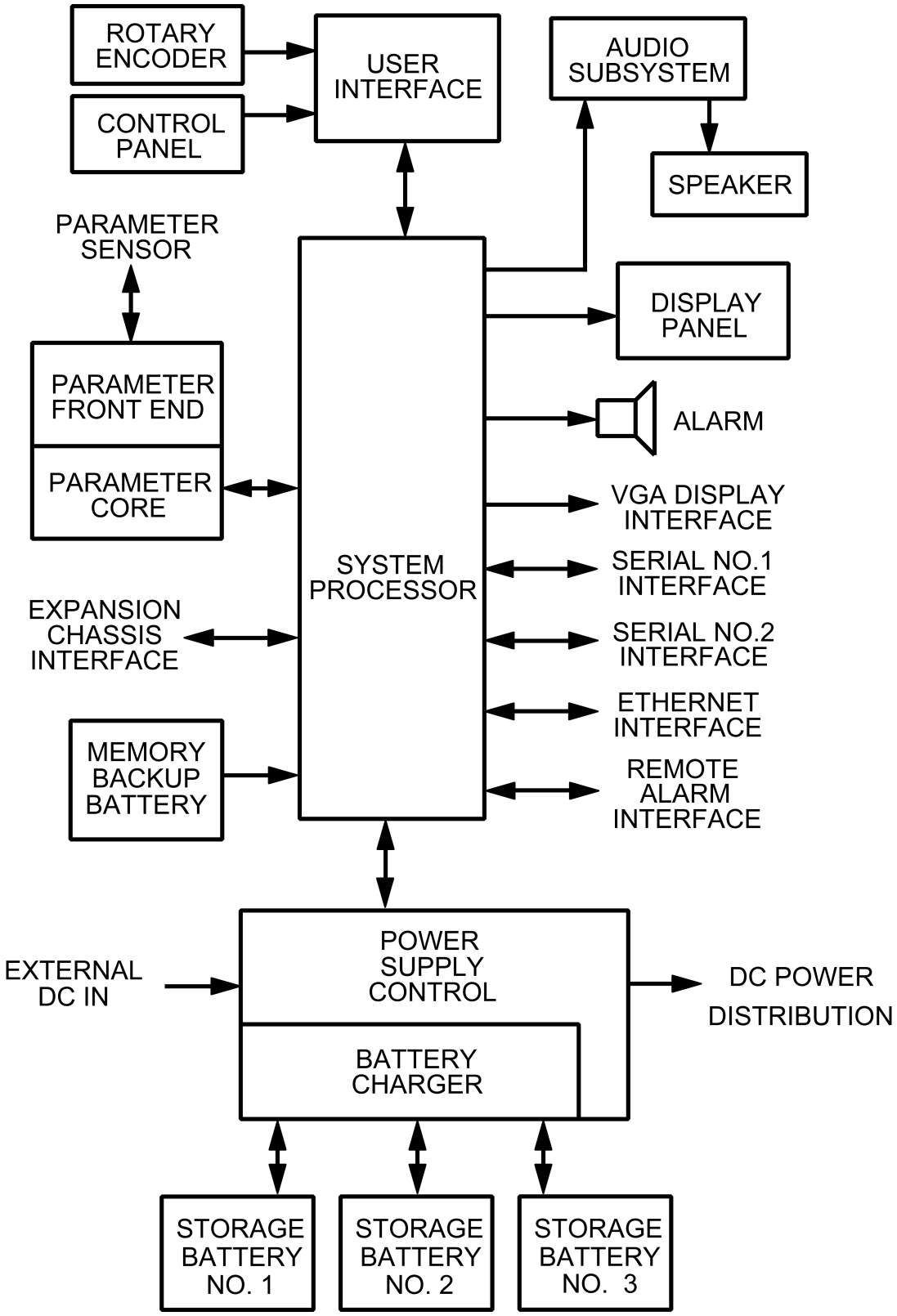
An overall block diagram of the Monitor is shown below. Functional block diagrams that provide major system operating details are described in the following paragraphs.

Data and Control Systems

FO-2A is a functional block diagram that ties together the two logical subsystems: the Patient Data System (PDS) and the Local User Interface system (LUI).

The PDS performs acquisition and storage of patient-specific data. Patient data are made available directly to the LUI, as well as other processes remote from the patient via a high speed communications port. The LUI is the mechanism which allows the caregiver at the patient to view and interact with the patient data.

The PDS comprises one or more Parameter Modules (PMs) and a Communications Processor (CP). The parameter modules provide the direct connections to the patient, and are each dedicated to one or more measurement functions. The CP coordinates communication among the PMs and prepares the data from the PMs for use by the LUI and remote users.



Overall Block Diagram

The LUI provides the display and user input at the monitor. The CP provides the highest priority of communications to the LUI, with guaranteed real time performance.

In the monitor, the CP and the LUI are physically implemented on a single processor system, with a direct connection to a video display and user input device.

The LUI and network users can determine what data are available from the PMs and request the data they need for display or storage. The CP then sends the data to the various users. In a stand-alone system the LUI simply displays the data from the patient as in a traditional monitor.

The PDS also supports trend data storage, power supplies, backup battery management, local recorder, and patient identification information.

Battery Regulator

FO-2B depicts the battery charger and power regulation circuits of the Monitor.

DC Power Paths

Voltage regulator circuits U14 and U27, at the upper right of FO-2B, provide four system operating voltages for the Monitor. The DCSOURCE input to the regulators can be provided by either external DC or (if external DC is not available) by a storage battery. The external DC input, from a provided inline AC power supply, is filtered by a protection circuit, and an LED lights to indicate that external power is available. EXT_DC_FILTERED is connected to DCSOURCE using FET switch Q21.

For ease of understanding, the three storage batteries are shown as a single block in FO-2B. The RAW_BATT output of each battery is connected to FET switches Q1 through Q6. When an output is selected, the FET switches connect the respective RAW_BATT output to DCSOURCE.

When acceptable external DC is present, battery power is not used, and boost regulator U20 is off. When a battery is the only power source, the boost regulator elevates the voltage of DCSOURCE to enable generation of the higher voltage outputs. When external DC is available, the battery charger circuit, comprised of U5, U10, and associated components, generates a VCHARGE output. FET switches Q7, Q11, and Q12 are used to apply VCHARGE to RAW_BATT of a selected battery.

Power Monitoring and Control

FO-2B depicts the power monitoring and control circuits that are mainly contained on the system support PWA, and shows how the circuits are linked to other Monitor components. Detailed descriptions of each PWA are provided in Component Principles of Operation.

Power regulator control is directed by PIC16C77 processor U23, an 8-bit CMOS device. Operating power for U23 is maintained by the PWR_MGR_5V supply. U23 monitors all major operating voltages. The three storage batteries are smart batteries that report temperature and charging status to U23. Analog switches U18 and U19 select the storage battery that communicates data with U23, and FET Q37 switches battery thermistor inputs to the U23.

I/O port expanders U17 and U24, controlled by I2C bus, extend the outputs of U23. The I/O expanders and analog switches communicate with U23 using the I2C bus. Demux U26 controls the FET switches. Counter U25 generates master clock PS_SYNC_CLK. Current sensor U21,U22 senses the current through DCSOURCE, and generates an I_DCSOURCE input to U23.

Primary CPU U30, on the system processor PWA, generates FS_PULSE via latch U6 whenever U30 is operating normally. The primary CPU also monitors the FS_FAILED and POWERFAIL outputs from the system support PWA.

TYPICAL PARAMETER MODULE OPERATION

A simplified block diagram of a typical parameter module is shown here. Each module is divided into isolated circuitry and non-isolated circuitry. The isolated circuitry includes the parameter sensor and the associated parameter front end. The isolated interface and DC-to-DC converter isolate this circuitry from the non-isolated parameter core logic that interfaces with the Monitor host.

Communication between the system host and Module is routed through the PNet synchronous serial interface, which also routes data acquisition and data processing commands to the parameter front end.

Isolated Circuits

Isolated module circuits are shown in the top half of the Typical Parameter Module diagram. An asynchronous serial communication channel isolates the core logic from the parameter front end. The isolated power block, typically consisting of isolated +15V, +5V, and -15V power supplies, provides operating voltages to the sensor connected circuitry.

Non-Isolated Circuits

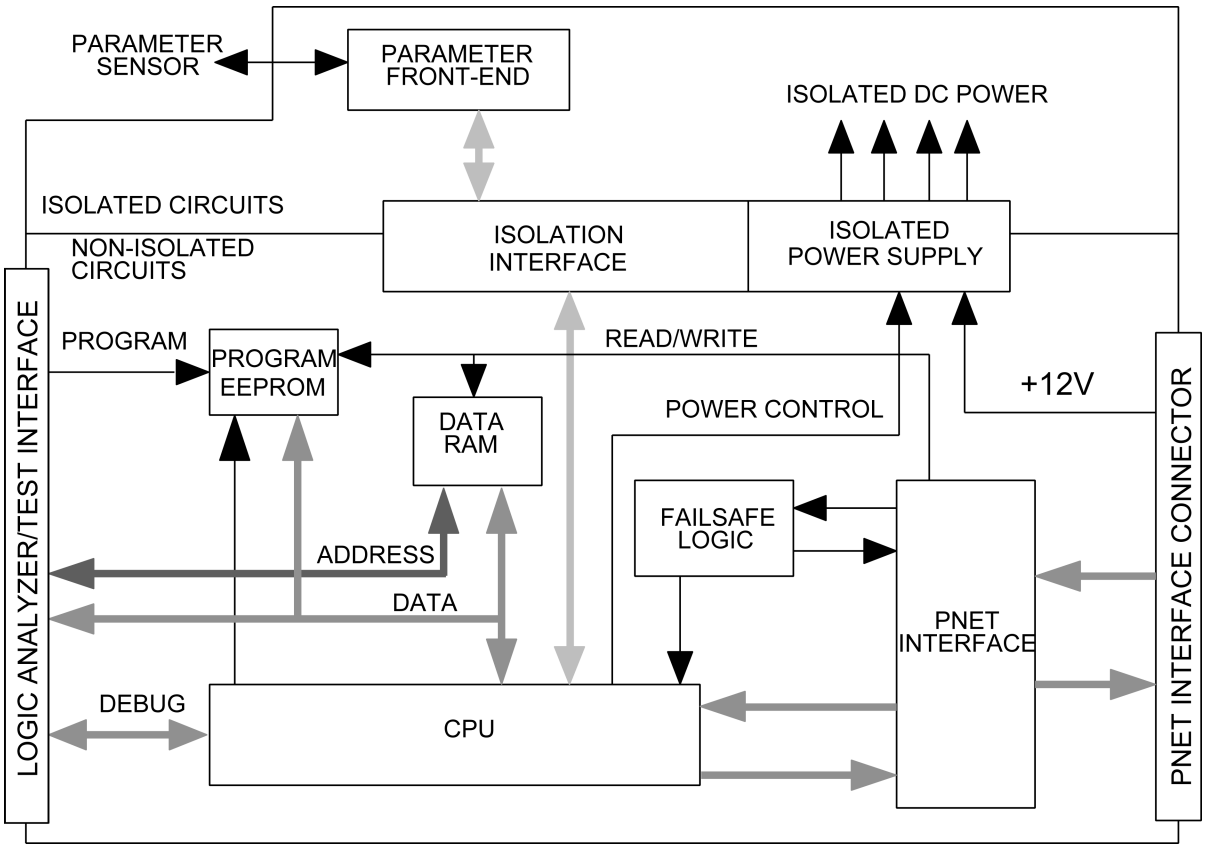
Non-isolated module circuits are shown in the bottom half of the Typical Parameter Module diagram. These circuits consist of the PNet interface, isolated power control, reset/failsafe, 68302 CPU, 128Kx8 data memory, 128Kx8 program memory, the model and serial number EEPROM, and logic analyzer/test interface. DC power is received through the Pnet interface connector, and applied to the isolated power supply. The supply powers the isolated circuitry after the CPU is reset, and shuts it down if a failsafe condition occurs.

Core logic power inputs to a typical module are limited to a peak inrush current during hot-plugging. Within 2 seconds the Module responds to identification and wakes up in a minimized power state until registered with the system.

The PNet interface provides asynchronous and synchronous data conversion between the microprocessor and the Monitor host. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor.

The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be reprogrammed through the PNET connector, or via the logic analyzer interface. Status and monitoring data is temporarily stored in the data memory for processing.

For further information about the unique operating principles of each of the interchangeable modules, refer to the modules index.



Typical Parameter Module

COMPONENT PRINCIPLES OF OPERATION

The following paragraphs provide a detailed component description of each of the major Monitor subassemblies.

System Processor PWA

The system processor PWA is a single board computer based on the Motorola MC68EN360 Quad Integrated Communications Controller (QUICC) and the MC68EC040 microprocessor. System processor PWA schematic diagram SC315-522 is provided within.

The board incorporates the following features:

- An 8-bit boot ROM
- A 32-bit-wide battery backed static RAM
- A 32-bit-wide flash program memory
- Address and data buffers
- Flat panel / CRT VGA video subsystem
- Battery backed real-time clock
- A 256 byte SPI compatible EEPROM
- P-net HDLC communications (SCC2) and parameter module selection logic
- IEEE 802.3 10BASE-T Ethernet port (SCC1)
- Asynchronous host communications interface (SCC3)
- Auxiliary serial interface/debug port (SCC4)
- Asynchronous user interface com. port (SMC1)
- Asynchronous audio processor com. port (SMC2)
- SPI compatible 8 - channel 10 bit A/D converter.

With the CPU board using the companion mode, the MC68EC040 processor uses the MC68360 as an intelligent peripheral providing memory control, interrupt vector generation, four serial communication controllers (SCCs), and two serial management controllers (SMCs) with UART capabilities.

The Motorola MC68EN360 (QUICC) Quad Integrated Communications Controller U30 is shown in sheet 1 of schematic SC315-522. The QUICC is comprised of three functional blocks:

- CPU32+ core
- SIM60
- CPM

With the MC68EC040 used as the primary CPU, the QUICC is in its companion mode as the communications processor module (CPM) and Intelligent I/O - Memory control module (SIM60). The MC68EN360 is a 32-bit CPU with 32 address and 32 data lines. It has dynamic bus sizing to accommodate 8, 16, and 32 bit ports. It does not have internal cache memory. The MC68EC040 is a 32-bit CPU with 32 address and 32 data lines. It does not have dynamic bus sizing capabilities. The MC68EC040 has a 4 kbyte instruction cache and a 4 kbyte data cache.

The QUICC memory controller has eight programmable chip-select pins for interfacing to memory and peripheral devices. The memory map for the CPU board and the associated chip-select assignments are shown in Table 2-1.

Table 2-1. CPU Board Memory Map

DEVICE		ADDRESS RANGE (hex)	PORT SIZE	QUICC CS~
Boot ROM	27C256	0x00000000 - 0x00007FFF	8	CS0~/CS5~
RTC	DS1284	0x00010000 - 0x000100FF	8	CS3~
Addr. Latch	HC259	0x00020000 - 0x0002003F		CS6~
QUICC internals		0x30000 - 0x31fff		
QUICC MBAR		0x0003FF00	32	
Flash ROM	29F010 x 8	0x00400000 -0x004FFFFF	32	CS5~/CS0~
Flash ROM	29F040 x 8	0x00400000 - 0x07FFFFF	32	
SRAM	TC551001 X 8	0x00800000 - 0x008FFFFF	32	CS4~
SRAM	TC554002 X 8	0x00800000 - 0x00BFFFFF	32	
VGA	primary	0x0C000000 - 0x0DFFFFFF	32	CS7~
DRAM SIMM (opt)	1 Mb x 36	0x0F000000 - 0x0F3FFFFF	32	RAS1

Clock Oscillator

As shown on sheet 1 of schematic SC315-522, clock oscillator U65 is a CMOS/TTL compatible device which provides a square wave output of 49.968 MHz. This signal is divided by two and buffered by flip-flop U23A to provide a 24.984 MHz square wave input to the QUICC clock synthesizer circuits and the BCLOCK input of the MC68EC040. The QUICC PLL clock synthesizer generates outputs CLOCK01 (the 24.984 MHz system frequency) and CLOCK02. CLOCK02 (49.968 MHz) is twice the frequency of CLOCK01 and is used by both the MC68EC040 PCLK input and FPGA U10.

Processor Configuration, Reset Strategies, and Boot ROM

In order to accommodate the ability to boot with either the MC68EN360 or the MC68EC040 as the primary processor and prevent the possibility of a "brain dead" system (in which the flash program memory has been corrupted), the following power-up sequence takes place:

- Upon power up, reset pulses are generated by the two power-up reset generator ICs, sheet 11 - U17 (MAX791A) and U41 (MAX701). These pulses are 200 ms long (minimum) and are adequate for resetting all ICs requiring reset input signals.

- When power is first applied, both the QUICC's RESETH~ pin and the MC68EC040 RSTI~ pin are held in reset by U17 and by gate pin U36-6, respectively. At the same time, D-flip-flop U37-B is reset causing the QUICC configuration input CONFIG2 to be held at logic high. This puts the QUICC in CPU32+ enabled mode for booting from an 8-bit device. U37-B also controls MUX U15 (sheet 4), enabling the global chip-select of the QUICC, CS0~, to select 8-bit boot ROM U51 at power-up.

- Boot ROM U51 is a 27C256R one-time-programmable device used for a power-on diagnostic analysis of flash ROM integrity before it is used as program memory. This approach prevents the possibility of a "brain - dead" system, since the boot ROM has flash ROM reprogramming capabilities.

At power-up, QUICC U30 boots from 8-bit boot ROM U51 in master mode while the MC68EC040 (U25) is held in reset mode (and consequently off the bus) by flip-flop U37A and U36-6. After the QUICC performs a checksum test to verify the integrity of the flash ROM memory, it will assert a general-purpose output bit (Port A-bit 15) RESET2~ to initiate a second reset. This second reset causes reset generator IC U17 to be activated and also sets flip-flop U37-B causing the CONFIG2 input of the QUICC to become low. The QUICC then exits reset in its companion mode, chip select mux U15 is configured to direct CS0~ to point to the 32-bit wide flashROM, and the MC68EC040 comes out of reset as the primary CPU.

Flash ROM Program Memory

The flash memory is selected by either the global chip select, CS0~, or CS5~ of the QUICC. This is controlled by Mux U15 based on processor configuration bit CONFIG2. In companion mode, CS0~ is routed to the flash memory in order to allow the MC68EC040 to boot from a 32-bit wide port. Inverter U22 provides further address decoding to provide a contiguous memory space for the flashROM banks. Both the address and data bus driving the flash memory subsystem are buffered by FCT buffer devices U70 and U66 (sheets 6 and 7).

The program memory is designed so its contents can be modified in-circuit. First-time programming can be performed with/without physically removing the devices from the PWB. This is to ensure that it is possible to reprogram the part without desoldering it from the PWB if a failure occurs during program transfer or upgrading.

Non-Volatile Battery Backed SRAM Banks

The battery backed SRAM banks are selected via a general-purpose chip select (CS4~) from the QUICC memory controller. This signal is routed to battery-backed microprocessor supervisory IC MAX791 U17 (sheet 11) for chip-select gating. The chip-select gating feature inhibits erroneous chip-select assertion during power failure conditions. The SRAM chip select (SRAM_CS~) is further qualified through battery-backed OR gate U9 to provide a contiguous memory space for the SRAM banks. Battery backed AND gates of U69 provide gating of the MC68EN360 WRITE_ENABLE signals and the R~_W signals for required memory control. Data memory is required to retain information when power to the MONITOR is removed. MAX791 U17 (sheet 11) enables the SRAM to be backed up by PWR_MGR_5V, a continuous 5V supply from the system support PWA. The supply is available under all normal and single-fault conditions.

Both the address and data bus driving the SRAM memory subsystem are buffered by FCT buffer devices U70 and U66 (sheets 6 and 7). The 70ns SRAMS require 1 wait state for proper timing operations.

Serial EEPROM

As shown on sheet 10 of schematic SC315-522, the CPU board includes 256 byte serial EEPROM U11 for storage of system parameters. This EEPROM is a Motorola Serial Peripheral Interconnect (SPI) compatible device. The interface to the processor is comprised of three signals from Port B of the QUICC (SPICLK, SPI_TXD, SPI_RXD) and a chip select signal (EEPROM_CS~) from bit 0 of addressable latch U7 (sheet 7).

The system software accesses the device by first generating the chip select (asserting EEPROM_CS~ low) and sending the appropriate address and command data to the chip using the internal SPI controller on the QUICC.

The hardware supports an SPI clock frequency of up to 1 MHz.

Address and Data Buffers

The address bus is buffered using FCT4X2244AT device U66. This device is 32-bits wide and is always enabled. The buffered address bus drives the flashROM, SRAM, bootROM, real-time-clock, and addressable latches.

The data bus is buffered using FCT4X2245AT device U70. This device is 32-bits wide and is enabled by the DATA_BUF_EN~ signal. This signal is generated by an output signal from FPGA (U10) if an appropriate chip select signal (SRAM_CS~, ROM_CS0~, CS3~, or CS5~) is present as an input. The direction of the data buffers is controlled by the processor R/W~ signal. The buffered data bus connects to the flashROM, SRAM, bootROM, and real-time clock.

Real Time Clock

As shown on sheet 7 of the schematic, the CPU board incorporates DS1284 single chip battery-backed real-time-clock U29. This device is memory-mapped and uses the CS3~ output of the QUICC as it's chip enable. This device is powered by PWR_MGR_5V to maintain the system timebase when external DC power is removed from the CPU board.

Video Subsystem

As shown on sheet 3 of schematic SC315-522, the CPU board includes a memory-mapped (using CS7~) video subsystem capable of simultaneously driving a CRT and a flat-panel display. The design provides drive for a 640 x 480 pixel flat panel EL/CRT display capable of displaying up to 256 colors.

The subsystem is made up of three main components: an FPGA, a CT65535 flat-panel video controller, and a 256K x 16 dynamic RAM.

The primary interface between the processor and the CT65535 is through the address and data buses (non-buffered). The data bus bytes are transposed to accommodate the Motorola/Intel byte ordering enigma.

CT65535 U20 is a VGA compatible, VLSI device which provides a bus interface, linear addressable display memory space, video memory refresh control, and flat-panel and CRT controller functions.

FPGA U10 is an EPM7032 EEROM based device. Its main function is to translate the MC68 bus signals into the required VESA VL-BUS V 1.0 compatible signals of the CT65535 video controller. The FPGA implements a state-machine driven by the CLK02 output clock signal (49.968 MHz) of the QUICC to generate the proper VL-BUS interface signals. The 256K x 16 DRAM U19 functions as the video display memory. It is accessed by the CT65535 for refreshing of the displays and accessed by the processor to change its contents. All processor video memory accesses and CRT refresh activities are managed by the CT65535.

The display drive signals are generated directly from the CT65535. The display drive and power signals leave the board via the display/user interface connector J5, and the CRT drive signals via connector J2.

Display power and brightness controls are provided and controlled via adressable latch U7 (sheet 7). Bit 3 (U7-7) is the DISP_12V_ON signal. When programmed to a logic high, the +12V supply for the flat panel display is turned on by MOSFET Q2 (sheet 16). MIC5014 U71 provides the high side drive for the FET. The BRIGHT_CONTROL signal is the output of X9312 50 kilohm EEPOT device U68 configured as a programmable voltage source. The EEPOT is controlled via latch U7 output bits 5, 6, and 7. It is software programmable by asserting its chip select U7-12, setting the up (1)/down (0) signal at U7-11 to the desired state and toggling INC~ at U7-10 the desired number of steps.

A/D Converter

As shown on sheet 10 of the schematic, the CPU board includes MAX192 8-channel 10-bit A/D converter U59. The A/D is a Motorola SPI compatible device, and is packaged in a 20 pin SSOP. The device is externally compensated, and generates a 4.096 Vdc reference internally. It is used in unipolar mode and therefore the scale factor is 4.096v/1024 ADU = 4mV/ADU. The interface to the processor is comprised of three signals from port B of the QUICC (SPICLK, SPI_TXD, SPI_RXD) and a chip select signal (AD_SEL~) coming from bit 6 of addressable latch U6 (sheet 7).

The analog input signals of the multiplexer and A/D converter are scaled by resistive dividers, with capacitors for low-pass filtering, before entering the chips. The voltage division brings each signal into the middle of the A/D dynamic range. The system software accesses the device by first generating the chip select by asserting AD_SEL~. Command data, indicating the channel to be converted, is then sent to the chip using the internal SPI controller on the QUICC. The A/D conversion result is clocked into the processor as second and third command bytes are transmitted.

The hardware supports an SPI clock frequency of up to 1 Mhz. This limit is throttled by the speed characteristics of the other SPI device (XC25C02). The hardware also supports continual system software reading of all channels of the A/D because the 1.5 microsecond acquisition time (taz) is absorbed during command byte transfer to the MAX192.

The analog input assignments for the A/D converter are as follows:

A/D channel	Signal
0	+5V ANALOG
1	+3.3 V
2	+12 V
3	CPU thermistor (100K)
4	-12 V
5	AG
6	I_SPKER
7	AG

IEEE 802.3 10 Base-T Ethernet Port

SCC 1 of the MC68EN360 has built-in Ethernet capability. Shown on sheet 9 of schematic SC315-522, SCC1 is programmed to run the IEEE 802.3 (Ethernet) protocol. This protocol is based on the carrier sense multiple access/collision detect (CSMA/CD) approach. The CPU board includes MC68160 enhanced Ethernet serial transceiver U18 to connect to the pulse transformer module and RJ-45 connector. The MC68160 performs the Manchester encoding/decoding and clock generation/recovery functions for the data link layer.

The differential output signals TXF, TXF~, RXF, and RXF~ are routed to connector J2 for further conditioning by the pulse transformer on the system support PWA. NOR gate U34C and AND gate U36D disable the Ethernet transmitter in the event of a FAILSAFE condition.

Parameter and Expansion Module Interface Hardware

Depicted on sheet 8 of schematic SC315-522, SCC2 of the CPU board has been designated for implementation of the RS-485 P-Net HDLC protocol, used for communications with the parameter modules. The CPU board supports the synchronous half-duplex implementation of P-Net in which the data and clock are generated at the data source. All control signals and RS-485 data/clock interface circuitry are resident on the CPU board. Baud rate generator No. 1 has been programmed to generate the P-Net transmit clock. This signal is converted to the RS-485 differential signals PNET_CLK+ and PNET_CLK- for transmission on the P-Net bus by U40. The P-Net receive clock is converted from RS-485 differential levels by U40 for reception on QUICC port A signal CLK3_PA10.

The transmission/reception functions for P-Net data transceiver U39 are transparently controlled by the PNET_RTS~ signal (port C bit-1 -> RTS~ of SCC2). Resistors R72 and R71 ensure that the P-Net_RX signal is in the idle line state in the absence of modules. Flip-flops U62 allow the P-Net Transmit Clock to continue for 4 cycles after P-Net_RTS~ is negated. This is done so that the 68302s in the parameter modules will get a timely receive interrupt.

The P-Net protocol is based on polling of the parameter modules on a scheduled basis. Each module is typically selected and queried for its data. The CPU board contains module selection and interface circuitry. The module selection logic is comprised of the 8-bit shift register latch 74HC595 U12. Six outputs of U12 form the MODULE_SELX lines for enabling each of the six parameter slots.

Additionally, the sixth bit of the shift register is buffered by U16 (EM_D) for output to the expansion module selection logic. Three general purpose I/O bits from the QUICC (MOD_DATA (port B - bit 12), MOD_LATCH (port B - bit 14) and MOD_CLOCK (port B- bit 13) are used for controlling the selection logic. MOD_DATA (=1) is shifted into the shift register (using MOD_CLOCK as the shift clock) until the desired module position is reached. MOD_LATCH is then asserted HIGH to latch the shift register data and select the desired module for polling.

The P-Net_RTS~ signal is buffered by NOR gate U34B and open-drain NAND gate U35B to generate the bidirectional TXOC~ signal, a control signal used to identify whether the source of the P-net message is in the chassis. P-Net input control signals M_SYNC and M_PRESENT are buffered by HCT244 U16 and passed to the QUICC on general purpose I/O port C bit 9 and port B bit 15, respectively. Additionally, P-Net control signal M_RESET is generated by the CPU on QUICC general purpose I/O port B bit-16.

The P-Net data, clock, and control signals are routed to both the P-Net backplane PWA via connector J7, and to the system support PWA via connector J2. The P-Net Clock signal is generated from the QUICC baud rate generator BRG01.

Asynchronous Serial Communication Channels

The CPU includes four asynchronous serial interface channels for communications with an external host computer, an auxiliary serial interface, and the PIC17C42 audio processor and PIC16C77 user interface microcontroller on the system support PWA.

These four channels are independently programmable and are directly supported by the QUICC serial communications controllers and serial management controllers. The user interface, audio processor, and ASI port have three wire channels TX, RX, and GND, while the host computer interface channel also includes the RTS~ and CTS~ handshake signals.

The audio, user interface, and ASI port signals are buffered and inverted by 74ACT540 device U8 (sheet 13) into CMOS compatible levels. The host computer interface signals are unbuffered and directly coupled to connector J2 for conversion to isolated (optocoupled) RS-232E signal levels on the system support PWA.

The QUICC communication channels, the corresponding CPU communications function, and suggested baud rate generator assignments are as follows:

COMM CHANNEL	CPU function	BRG
SCC1	Ethernet	N/A
SCC2	P-Net	BRG01
SCC3	Host Port	BRG04
SCC4	ASI Port	BRG02/BRG03
SMC1	User I/F	BRG02
SMC2	Audio Proc.	BRG03

Parallel I/O Ports and Addressable Latch Pin Functions

The QUICC contains three general purpose I/O ports as part of its communications processor module (CPM). Port A, port B, and port C have multifunctional pins which are controlled by the system software. Additional output bits have been provided by 74HCT259 addressable latches U6 and U7.

Audio Processor

Microcontroller U31 (sheet 12) provides arbitrary waveform sound playback capability. Crystal Y2 sets the operating frequency of the internal oscillator to 15.928 MHz. Audio processor U31 reset is provided by the system processor MTR_RESET~ input. The PIC17C42 processor is operated in the extended microcontroller mode. This mode uses 2K words of internal ROM, 256 bytes of internal RAM and provides an address space of 62K words for external RAM.

A full duplex asynchronous serial data interface provides communication between U31 and the primary CPU. This interface allow commands to be sent to the software running on U31 and status information to be transmitted back to the primary CPU. An on-chip UART provides this interface. The data inputs and outputs are buffered by U8 (sheet 17) to protect U31.

U31 interfaces to 128K x 16 bits of flash memory, U4 and U5, via a 16 bit multiplexed address/data bus. Latches U2 and U3 latch the address during the first part of the memory cycle. Data is read or written during the second half of the cycle. The instruction cycle time at a clock of 15.928 MHz is 251 nsec. External memory occupies addresses 0x0800 - 0xFFFF. Lower addresses are in the on-chip ROM program memory. Addresses lower than 0x0800 in the external memory are not accessible. Since the 16 bits of address data can only address 64K, an additional address bit is provided as a bank select signal from U31 output RB7.

Data for the DAC is latched in the same manner as the flash memory data. To prevent interaction between DAC write cycles and memory write cycles, separate enable signals are provided to select the write mode. U31 outputs RB6 and RB3 respectively enable flash U4 and U5. RB5 enables the DAC and DAC latch U32. In operation, the flash is enabled only during flash memory accesses and the DAC latch enabled only during DAC accesses. A write to any address greater than 0x7FF will latch data into the DAC latch. AUDIO_ON (RB4) via Q4 is used to activate U33, a switch to connect or disconnect the speaker.

Sound Generation

The audio processor enables the generation of programmable arbitrary waveforms at a software selectable volume. U27 is a 12 bit parallel input multiplying DAC configured to generate a bipolar output signal. Data input to the DAC is provided by DAC latch U32. The output amplitude for a given code is proportional to the reference voltage. For bipolar operation, the DAC requires equal positive and negative reference voltages. A variable reference voltage is provided from a programmable pulse width modulator (PWM) built into U31 (RB2). The PWM can generate a 0 - 5 volt reference with 8 bit resolution. The PWM output is filtered by low pass filter C115 and R90. U24 buffers the reference voltage and provides the inverted and non-inverted references to DAC U27. In operation, the overall audio output amplitude is controlled by varying the DAC reference voltage.

The output of the DAC is filtered by a Chebyshev 0.1 dB ripple three pole low-pass filter U24 and amplified by bridge-tied-load power amplifier U38 to a level appropriate to drive the speaker. The filter cutoff frequency is set to 5 kHz, and provides an attenuation of 15 dB at the sampling frequency of 11 kHz. The low pass filters roll-off the amplifier gain at post-audio frequencies to eliminate oscillation.

FET U33, controlled by the signal AUDIO_ON, allows disconnecting the speaker from the amplifier. U33 is an enhancement mode FET, and requires that the gate be more than +5 volts with respect to the source when ON. Gate drive is provided by a bootstrap technique to allow the switching of 12 volt positive voltages with only a 5 volt supply. Each output of amplifier U38 is biased at about +6 Vdc with no signal output. Each output varies symmetrically above and below +6 Vdc during sound generation. To turn on the transistor, the input of R56 is driven to +12 Vdc. Thus, the average voltage on U33-S is +6 volts, while the average voltage on U33-G is +12 volts. The high impedance of R56 and the low impedance of C94 at audio frequencies causes the gate drive to follow the source drive and maintains a +6 volt Vgs on U33, keeping the FET on. Similarly, driving R56 to ground keeps U33 off. Q14 amplifies the logic level input AUDIO_ON to the required 0-12 Vdc level shifted levels.

Speaker Current Sense

The speaker current is monitored to verify the speaker is drawing current and is not damaged. This is accomplished by monitoring the input current to the power amplifier. The current used by the audio amplifier is monitored, and a proportionally conditioned DC voltage is generated and sent to the system processor.

SYSTEM SUPPORT PWA

The system support PWA contains power supply circuits accomodating external DC input and intelligent battery selection, operation, and charging. User interface functions include keypad scanning, keypad backlighting, select knob encoding, power supply indicator drivers, and status indicators. The PWA also contains the Ethernet interface, isolated SERIAL #1 interface, SERIAL #2 interface, expansion module connector interface, VGA video filters, and remote alarm controller, and provides interface to the IOCA PWA and ON/OFF switch and indicators. Refer to system support PWA schematic diagram SC315-524.

Uninterrupted DC

As shown on sheet 1 of SC315-524, the power inputs (RAW_BATT 1, 2, &3 and SYS-12V) are diode ORred together to give UNINTERRUPTED DC. UNINTERRUPTED DC is then used as the input to the VGATE charge pump, the PWR_MGR_5V regulator and the AUX_12V regulator. In addition to the GF1A used to diode OR the inputs together, series regulator U31 is used on the EXT_DC_FILTERED input to limit UNINTERRUPTED DC to 18 V maximum.

VGATE is generated with ICL7662 voltage converter U8 configured as a voltage doubler and is enabled via the CMOS GATE_VOLTS_ON signal generated from the PIC16C77 U23 via I2CBUS I/O port Extender U17. Transistor Q25 turns on series pass transistor Q26 to enable the VGATE signal.

Linear regulators are used for AUX_12V and PWR_MGR_5V. Fixed linear regulator U7 generates PWR_MGR_5V, and an adjustable linear regulator is used to generate AUX_12V. UNINTERRUPTED_DC and 9VBATT are diode OR'd to provide input for PWR_MGR_5V the regulator. Because the SYS_12V buck regulator is more efficient than the AUX_12V linear regulator, SYS_12V is connected to AUX_12V through a diode. The reverse leakage current of an LT1121 is specified at 25uA maximum.

Microcontroller Functions

Microcontroller PIC16C77 is an 8-bit CMOS device with an 8192-word program memory and 192 bytes of RAM and several integrated peripherals (schematic sheet 2). The peripherals used in the design of the SSSB include the two PWM (pulse width modulated) output pins with 10 bit resolution, an 8 channel 8-bit A/D, a full duplex asynchronous communications I/F, an I2C compatible synchronous serial interface, and several general purpose I/O pins.

The processor has a micropower sleep mode that is utilized by design on the SSSB. On the SSSB the PIC16C77 processor clock speed is 8.622MHz.

The hardware subsystems controlled by the PIC16C77 include on/off button management, smart battery charger/selector/host intelligence, keypad scanning/backlighting and rotary encoder knob decoding, power system control, and fault alarm generation.

Signal BUTTON_DWN~ (U24-12) is generated by the momentary on/off switch connected at P6 (sheet 11) and causes an interrupt to the PIC16C77 at RB4 (U23 pin 14) and causes it to WAKEUP. When EXT_DC_FILTERED is available, the engagement of the SelectKnob will do the same via the KNOB_PUSH~ signal (U23 pin 42) generated on the user interface PWA (the PIC16C77 Port B4 to PortB7 pins cause an “interrupt-on-change”). The remaining “interrupt on change” pins are connected through external Schmitt trigger buffers and are assigned to the SelectKnob rotary encoder signals PHASEA and PHASEB for the decoding.

Table 2-2 lists the I/O signal definitions and assignments for the PIC16C77, and Tables 2-3 and 2-4 list them for its companion PCF8574 I2CBUS I/O port expander ICs U17 and U24.

Table 2-2. Microcontroller Signal Definitions and Assignments

Pin Name	Assignment	I/O	
RA0/AN0	9VBATT	analog_in	9V battery voltage
RA1/AN1	I_DCSOURCE	analog_in	Current drawn from DCSOURCE
RA2/AN2	DCSOURCE	analog_in	DCSOURCE voltage
RA3/AN3	TEMP1	analog_in	Thermistor for RAW_BATT1
RA4/T0CKL	SMB_EN	0	Enable SMBus
RA5/AN4/SS~	TEMP2	analog_in	Thermistor for RAW_BATT2
RE0/RD~/AN5	TEMP3	analog_in	Thermistor for RAW_BATT3
RE1/WR~/AN6	EXTERNAL_DC_FILTERED	analog_in	External DC supply voltage
RE2/CS~/AN7	VCHARGE	analog_in	Battery charger current voltage

Table 2-2. Microcontroller Signal Definitions and Assignments (Continued)

Pin Name	Assignment	I/O	
RC0/T10S0/T1CKL	9V_STRB	O	Polls the 9V battery voltage
RC1/T1OSI/CCP2	CURRENT_PWM	O	PWM controlling charger current
RC2/CCP1	OFF_GATE	O	PIC output to the FS PLD
RC3/SCK/SCL	I2CCLOCK	I/O	I2C bus clock signal
RC4/SDI/SDA	I2CDATA	I/O	I2C bus data signal
RC5/SD0	FS_WDOG	O	Output to FS circuitry
RD0/PSP0	CBSA	O	Charge Battery Select A
RD1/PSP1	CBSB	O	Charge Battery Select B
RD2/PSP2	FS_TEST	I	Input from the FS PLD
RD3/PSP3	KEY5	I	Keypad matrix input
RC6/TX/CK	UI_RX	O	Data transmitted to CPU UI port
RC7/RX/DT	UI_TX	I	Data received from CPU UI port
RD4/PSP4	KEY1	I	Keypad matrix input
RD5/PSP5	KEY3	I	Keypad matrix input
RD6/PSP6	KEY2	I	Keypad matrix input
RD7/PSP7	KEY4	I	Keypad matrix input

Table 2-2. Microcontroller Signal Definitions and Assignments (Continued)

Pin Name	Assignment	I/O	
RB0/INT	POWERFAIL~	I	SSSB hardware detected power failure
RB1	USBA1	O	Control output for battery switch 1
RB2	USBA2	O	Control output for battery switch 2
RB3	DCSEN~	O	DCSOURCE enable
RB4	INT from U24	I	Input I2C peripheral U24. Includes BUTTON_DWN~
RB5	KNOB_PUSH~	I	Input from SELECT KNOB
RB6	PHASEA	I	Input from SELECT KNOB
RB7	PHASEB	I	Input from SELECT KNOB

Table 2-3. Port Expander U17 Signal Definitions and Assignments

Pin Name	Assignment	I/O	
P0	GATE_VOLTS_ON	O	Enables VGATE
P1	PS_SYNC_EN~	O	Enables power supply sync clock
P2	THERM_EN~	O	Enables PIC to derive temp readings of batteries
P3	CHARGER_ON~	O	Control output to enable battery charger
P4	SERVICEMODE	O	Output signal to CPU for SERVICEMODE
P5	FAN_ON	O	FAN control signal
P6	CHARGE_EN	O	Enables PIC to control battery charger switches
P7	PWR_SYS_ON	O	Control output to enable system power regulators

Table 2-4. Port Expander U24 Signal Definitions and Assignments

Pin Name	Assignment	I/O	
P0	SMB_SELA	O	Signal to select smart battery for SMBus COMM
P1	SMB_SELB	O	Signal to select smart battery for SMBus COMM
P2	EXT_DC_LED	O	Activates EXT DC LED
P3	CHARGE_LED	O	Activates charge LED
P4	STAT_DC	O	Control output to illuminate battery operation LED
P5	SLEEP	O	Asserted to FS circuitry when PIC is in SLEEP mode
P6	EX_DC_AVAIL~	I	Interrupt to PIC on EXT_DC becoming available
P7	BUTTON_DWN~	I	Interrupt to PIC on button being pushed

The PIC16C77 (U23, sheet 2) is always powered by the PWR_MGR_5V supply. This supply is generated by a LT1121CST-5 linear regulator (U7, sheet 1). When the Monitor is OFF and no external DC is available, the PIC will reside in its low-power SLEEP mode and draw only 40 uA. The PIC16C77 is initially reset by its on-chip power-on reset generator.

The PIC16C77 performs (as a minimum) the following sequence to ensure minimal power consumption before entering SLEEP:

De-asserts the GATE_VOLTS_ON signal,

Disables the charger switches by driving the CHARGE_EN~ signal. The outputs of the 2-to-4 decoder are driven high to prevent battery charge switch selection, and

Disables DCSOURCE by driving the DCSEN~ signal. The outputs of the 2-to-4 decoder are driven high to prevent battery charge switch selection.

Additionally, upon WAKEUP, the PIC16C77 performs (as a minimum) the following sequence before engaging battery charger operation or battery switching:

Asserts the GATE_VOLTS_ON signal to turn the VGATE supply on,

Evaluates the available power sources including RAW_BATT1, RAW_BATT2, RAW_BATT3, and external DC,

Enables charger switch operation and DCSOURCE by asserting DCSEN~ and CHARGE_EN, and selects switches as needed to power system and charge batteries, and

Awaits interrupt from POWER SWITCH.

PIC16C77 U23 controls the application and generation of regulated system power to the Monitor. Additionally, the PIC16C77 monitors the external DC input and up to three SMBus compatible nickel metal hydride (Nimh) batteries.

U5, an LT1511, is a constant current/constant voltage PWM current mode controller with built-in 3 Amp pass element. The charger IC is powered by the EXTERNAL_DC_FILTERED supply. The charge current is programmed by the PWM output bit of the PIC16C77. PWM1 (U23-18) controls the charge current by adjusting the current drawn from the LT1511 PROG pin (U23-19) with Q44.

The PIC16C77 can selectively enable/disable the charger using Q34 via the CHARGER_ON~ signal. This signal is diode-OR'd with FS_FAILED, which also has control of charger operation. FS_FAILED also places the PIC16C77 in hardware reset via Q46.

The PIC16C77 I2C bus interface is the SMBus communication vehicle. The PIC16C77 can selectively transmit/receive commands to/from any of the three smart batteries in the system. The PIC continually monitors the smart battery SMBus communications to establish safe charging approaches. Smart battery data and capacity information are transmitted to the system processor upon request or as initiated by the PIC.

Power Switches and Powerfail

Sheet 3 of SC315-524 shows three sets of battery switch networks designed to connect any of the three system batteries to the DC_SOURCE power bus or to the battery charger output. It also shows the switch for EXT_DC_FILTERED and the POWERFAIL circuitry.

In normal operation, the PIC16C77 allows the system to run either on a battery or the EXTERNAL_DC supply (if present).

Two-to-four decoder U26 connects the PIC16C77 to the control signals for each battery charger power MOSFET (Rdson = 0.0135 ohms max). Diodes CR9, CR43, and CR44 prevent the body diode of the power FETs from conducting in the absence of system power. The 15V Zener diode limits the Vgs of the Si4412DY MOSFET.

The battery switches to DCSOURCE are Q2/Q5, Q3/Q6 and Q1/Q4, power MOSFETs with an Rdson of ~13.5 mOhms. A back-to-back FET design is used to prevent reverse powering of the batteries through the body diode of the top FETs. These power FETS are connected (through buffers Q14, 23, and 11) to a 2-to-4 decoder (U26, pins 5, 6, and 7) that allows the PIC16C77 to control battery switching. The 15V Zener diode limits the Vgs of the Si4410DY MOSFETs.

Q21 (IRLZ44S, Rdson = 0.028ohms max) is connected to the same 2-to-4 decoder as the battery switches and is used to switch to EXT_DC_FILTERED as the input for DCSOURCE. rectifier CR8 prevents reverse feeding of EXT_DC_FILTERED through Q21.

A MAX472 (U21) is used to sense the current through DCSOURCE. This allows comparator U22 to see when the primary power source has been disconnected and assert the signal POWERFAIL~. This signal is used by the PIC16C77 to switch to another power source without interruption of system power.

The output of the MAX472 is a dependent current source with the gain set by sense resistor R11 and gain resistors R112 and R49. To prevent voltage saturation of the MAX472 output stage, a two stage gain network is implemented with R104, R186, and CR61. The output is then directly used by comparator U22 to generate the POWERFAIL~ signal. The gain for the A/D signal I_DCSOURCE is set by R104.

Boost Converter

The battery boost converter is shown in the upper left of schematic sheet 4. The boost converter boosts the DC_SOURCE Bus to ~15.5V. When the monitor is powered by EXTERNAL_DC the boost converter is effectively shut down and the boost converter output is the DC_SOURCE value (less the drop across CR41 and loss thru L4). The boost converter converts the battery voltage of +10V to +14V to +15.8V for the SYS_12V buck regulator. This +15.8 V output is maintained even if the battery voltage falls to +10V.

Current feedback to U20 is provided by current transformer T4, via diode CR35. Voltage feedback is provided by voltage divider R75 and R82, whose values set the regulated output voltage to 15.8 volts nominal. The oscillator in U20 is synchronized to the master clock by clock signal PS_SYNC_CLK generated by counter U25 (sheet 2). The absence of the PS_SYNC_CLK signal prevents the boost from operating.

SYS_12V

The SYS_12V supply is generated using current mode controller U27. This is a PWM buck topology, and its input voltage is the output of the boost regulator stage. U27 uses power switch Q40 and synchronous rectifier Q41 to achieve high efficiency.

U27 is a monolithic voltage-mode PWM regulator IC with internal clock, error amplifier, reference, current sense logic, and dead-time logic. Output voltage is set by feedback divider R48 and R105.

U27 generates the high-side drive (via internal charge pumping through diode CR40 and capacitor C94) for Q40 and the needed drive current for synchronous rectifier transistor Q41, from the complementary outputs of U27.

Output current is sensed by R98 in series with the load. This sense voltage is fed back to U27 via dividers R134/R41 and R105/R48. The internal clock of U27 is internally synchronized to the 296 KHz signal PS_SYNC_CLK.

SYS_3.3 V and SYS_5V

This section is a dual channel buck regulator that generates the logic output voltages from the DC_SOURCE voltage input.

U14 is a dual PWM switching regulator controller. Using external MOSFETs Q39/Q32 and Q27/Q19, the circuit efficiently generates +3.3 and +5 volts respectively from varying input voltages.

U14 provides separate pulse-by-pulse current limiting for each output. Current sense resistor R74/R83 set the limit for the 5 volt output, while R50 sets the limit for the 3.3 volt output. The internal clock of U14 is internally synchronized to the 269 Khz signal PS_SYNC_CLK.

SYS_-12V

Step-up transformer T3 and half bridge rectifier CR63 and C45 use the switching voltage at the input to the SYS_12V inductor to generate about -14V. Linear regulator U16 then regulates this voltage to create SYS_-12V.

Power Supply Protection

As shown on schematic sheet 11, overcurrent protection is provided by fuse F1.

VGA Filters

The system support PWA provides impedance matching and filtering for the VGA signals RED, GREEN, and BLUE from the system processor (sheet 9). The HSYNC and VSYNC signals are filtered and are OR'd with FS_FAILED through U12.

User Interface

A full duplex asynchronous serial interface provides communications between U23 and the primary CPU on the system processor PWA. This interface allows commands to be sent to the software running in U23 and status information to be transmitted back. An on-chip UART provides this interface. The data inputs and outputs are buffered by transistors Q30 and Q38 (sheet 10) to protect U23.

Ethernet Interface

An isolated 10-BASE-T Ethernet interface (schematic sheet 9) is provided to connect the Ethernet circuitry on the system processor PWA to the Ethernet connector. T2 provides the dielectric isolation for the Ethernet port, as well as the common mode choke and the data bandpass filters. Signals are provided to drive LEDs that indicate RXD, TXD, and link integrity status. R95, R96, and R135 provide current limiting for these LEDs.

Serial No. 2 Interface

A buffered bidirectional serial port is provided by the system processor PWA. These signals pass through the system support PWA to the external connector. CR26, CR42, R99, R128, and R69 provide overvoltage and overcurrent protection for the serial communication lines. The system 5 volt power is supplied to the port through PTC4, which provides overcurrent protection.

Serial No. 1 Interface

Isolation and signal level conversion is provided for an RS-232 compatible full duplex asynchronous communication port (schematic sheet 8). The interface provides the signals TxD, RxD, CTS, and RTS for modem interface capability. Data rates up to 19.2 Kbaud are supported. A push-pull isolated power converter is created by U9 and T1. The outputs of T1 are then rectified by U30 to give +5_ISO. Optocouplers U1, U2, U3, and U4 isolate the 4 data lines. The optocouplers provide 2500 Vrms isolation to the serial port. The input LEDs to the couplers are driven by logic level FETs through current limiting resistors to provide adequate LED drive. RS-232 level converter U6 translates between the logic level signals at the opto-couplers and RS-232 voltage levels at the port connector.

Alarm Tone Generator

The failsafe circuitry (sheet 5) is designed to insure failsafe alarm operation under all normal and single fault conditions.

An asynchronous state machine is implemented in the PLD. It uses input signals WDOG_OK~, BD, SYS_5V~, SLEEP, and OFF_GATE to control the FS sounder. WDOG_OK~ is asserted when the PIC toggles the FS_WDOG line at >1kHz. Signals BUTTON_DWN~ and SYS_5V are run through schmitt triggers to create BD and SYS_5V~; this is done to meet the rise time requirements of a zero power PLD.

When the PLD asserts the FS signal (low) Q31 is turned on applying power to U15. U15 is configured as a square wave oscillator operating at approximately 700 Hz, the optimum frequency for the alarm speaker. Q20 is configured as a current source which drives the alarm speaker and is controlled by the oscillator output. R125 sets the speaker current, which is independent of the unregulated input voltage.

Power Supply Status Indicators

Q8, Q9, and Q15 (schematic sheet 7) interface the control signals from the system support PWA to the LED indicators on the front of the instrument. When EXTERNAL_DC is available for operating the instrument, the AC LED is lighted through current limiting resistors R12 and R13.

When the instrument is operating on battery power, Q15 drives the BATTERY LED via current limiting resistors R26 and R168. When the battery is charging, CHARGER_LED is asserted and Q9 drives the CHARGE LED through current limiting resistors R19 and R20.

Expansion Connector Interface

The expansion connector signals are passed through from the system processor PWA through the system support PWA to the external connector. Logic power is provided to the expansion connector through PTC3, which provides overcurrent protection, while FB5 and associated parts provide EMI filtering.

Remote Alarm Interface

A relay interface (sheet 6) is provided for hard-wired communication of alarms. The interface comprises a logic signal provided as a single-pole-double-throw relay contact set. The customer may connect to either the normally-closed or the normally-open set of contacts, depending on the interface requirements of his associated equipment. Software in the monitor will allow configuring the monitor to activate or de-activate the relay in the event of an alarm condition. Different alarm assignments may be provided by the monitor software.

The interface consists of three terminals: COMMON (COM), NORMALLY-OPEN (NO), and NORMALLY-CLOSED (NC). The contacts are arranged so that there is always continuity from COM to one of NO or NC, but never both. When the monitor is not operating (powered OFF), there is continuity between COM and NC to indicate operational status. During normal operation in the absence of an alarm condition, there is continuity between either COM-and-NC or COM-and-NO, depending on the software setup. The appearance of an alarm condition, as defined by the software setup, will cause the continuity to switch to the opposite contact. Short circuit protection is provided by overload protector PTC2.

USER INTERFACE PWA

The user interface PWA provides the keypad switches, LED backlighting, and optical encoder interface for the Monitor. The user interface PWA interfaces with the PIC16C77 power supply and user interface processor on the system support PWA.

The user interface PWA interfaces and decodes 5 keys with a 3-column-by-2-row configuration. The columns are asserted one at a time, and the rows are sampled to obtain the correct key. The keypad signals are then decoded by the PIC16C77 and communicated to the MC68EN360 on the system processor PWA. Refer to the user interface PWA schematic diagram SC315-530.

The front panel optical encoder produces 2-bit quadrature pulses. The encoder output is conditioned by Schmitt inverter U29 on the system support PWA. Encoder de-bounce is accomplished by software. Each change in position is communicated to the system processor.

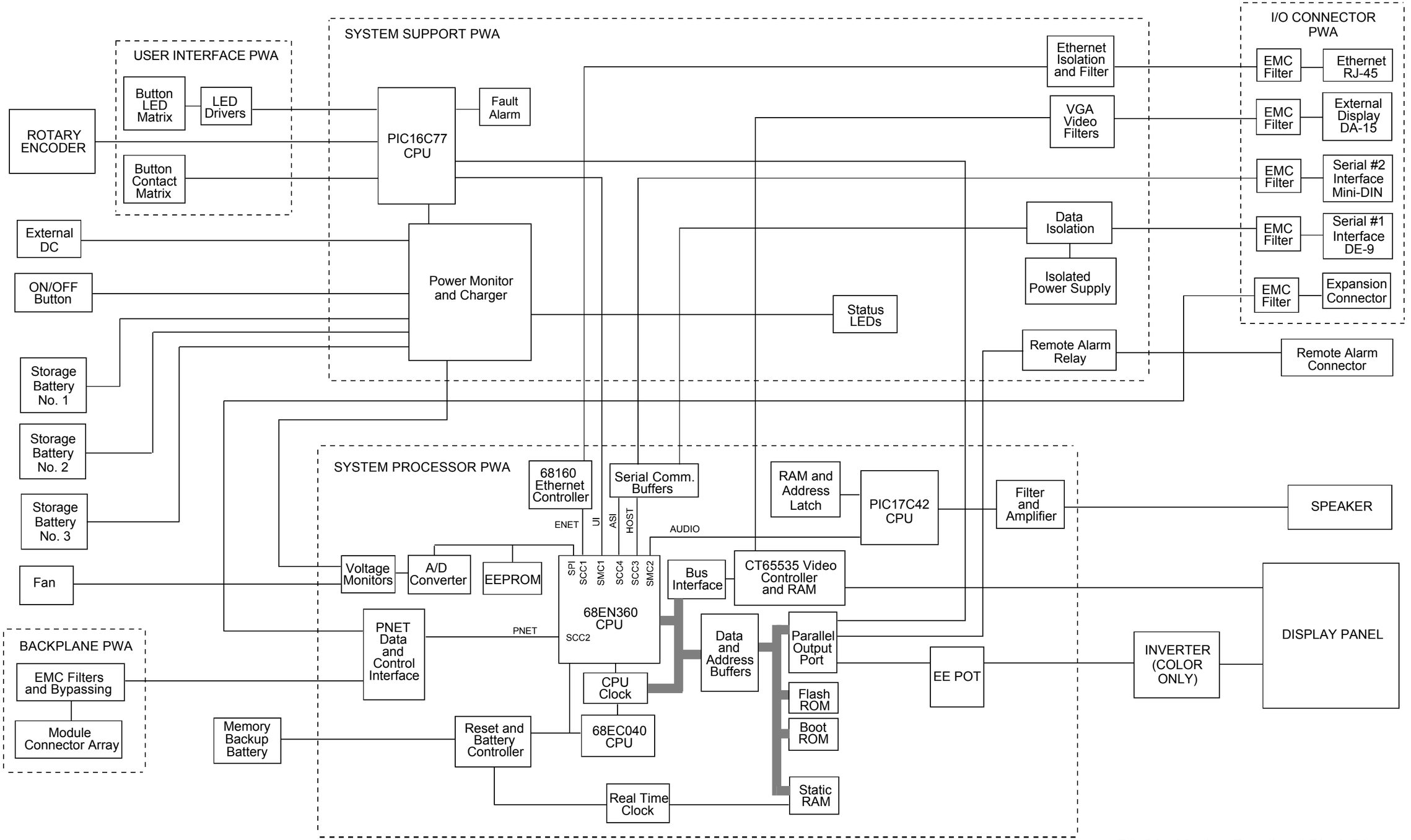
The user interface PWA drives five dual color (green, orange) LEDs. U1 and U2 are I/O expanders driven from the I2C bus 2-wire serial interface of the system support PWA PIC16C77. These devices are configured as I2C bus addresses 0x40 and 0x41. Each indicator contains two different color LEDs for keypad key backlighting. An optional yellow color is formed when both LEDs are lighted. The red alarm LED is brighter than the other LEDs.

BACKPLANE PWA

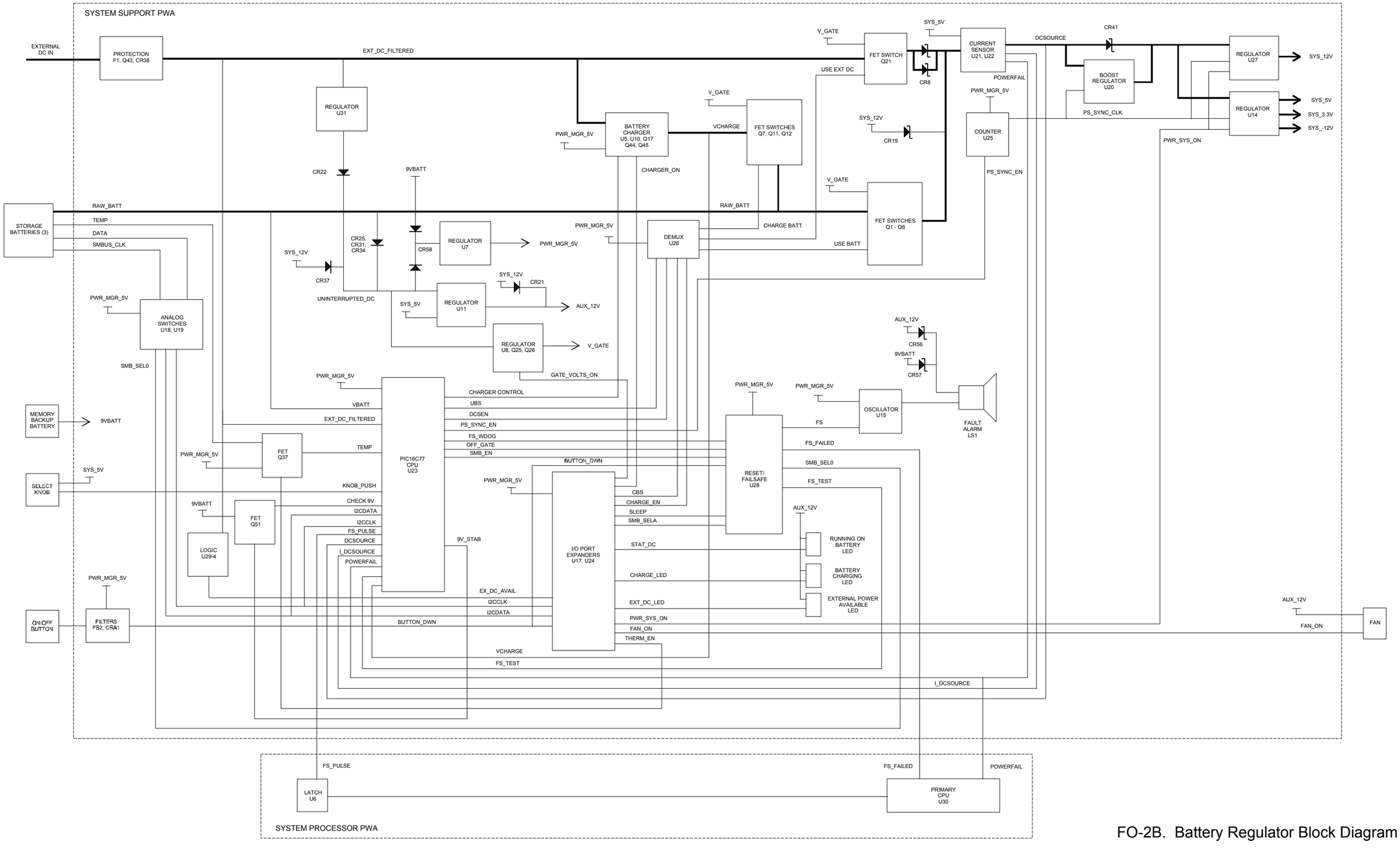
The backplane is the connector PWA into which the parameter modules plug. It connects the module interface signals from the system processor PWA to the parameter modules, and supplies power to the modules from the power supply. The backplane assembly includes the cast metal bulkhead which provides mechanical rigidity for the connectors, alignment features for module installation, and EMI shielding. The backplane PWA provides connectors for six parameter modules. Refer to the backplane PWA schematic diagram SC315-523.

Independent passive LC filters are provided for the +3.3V, +5.0V, and +12.2V supplies at each module connector. These filters prevent the hot-insertion of a module into a slot from corrupting the supplies to the other modules or the system. This limiting action also protects the connector contacts.

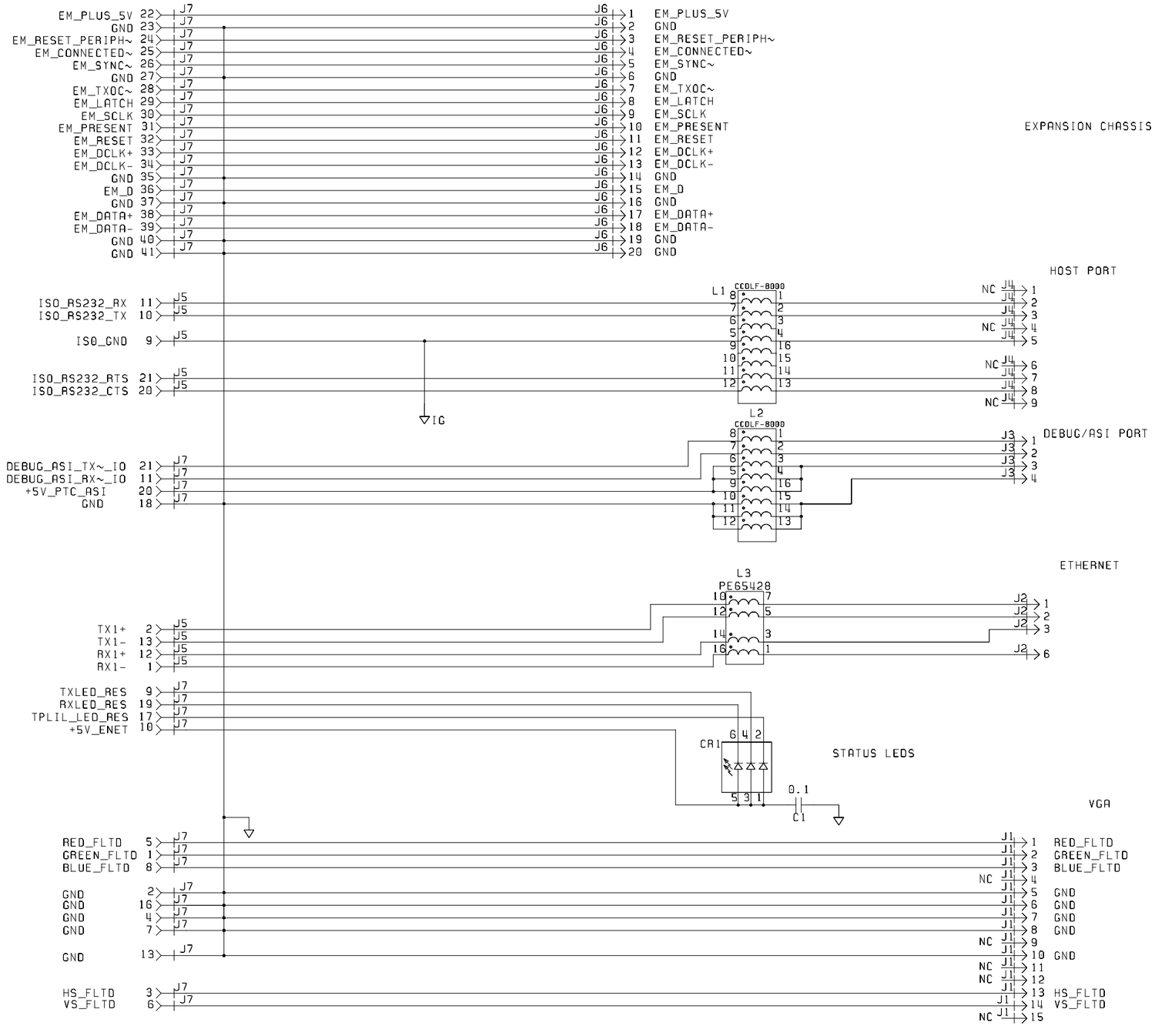
The board contains four layers. Layer 1 is a ground plane which aids in EMI shielding of the module bay. Layer 2 provides planes for the distribution of the +5 Volt and +12 Volt system voltages. Layers 3 and 4 are used as signal layers for the module control signals, as well as distribution of the -12 Volt and +3.3 Volt system supplies.



FO-2A. Monitor Functional Block Diagram



FO-2B. Battery Regulator Block Diagram

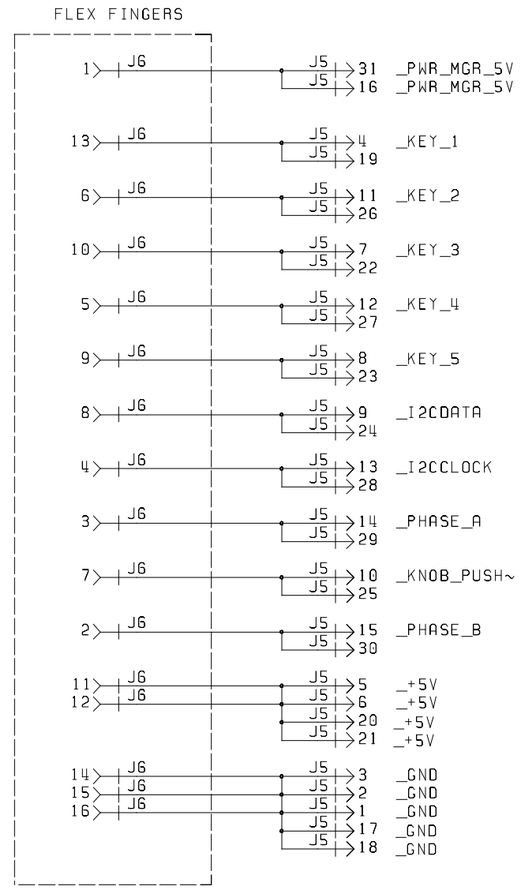


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%, 1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C1, CR1, J7, L3
   B. REFERENCE DESIGNATORS NOT USED:
      NONE

SC313-117 A
IOCA Flex PWA Schematic

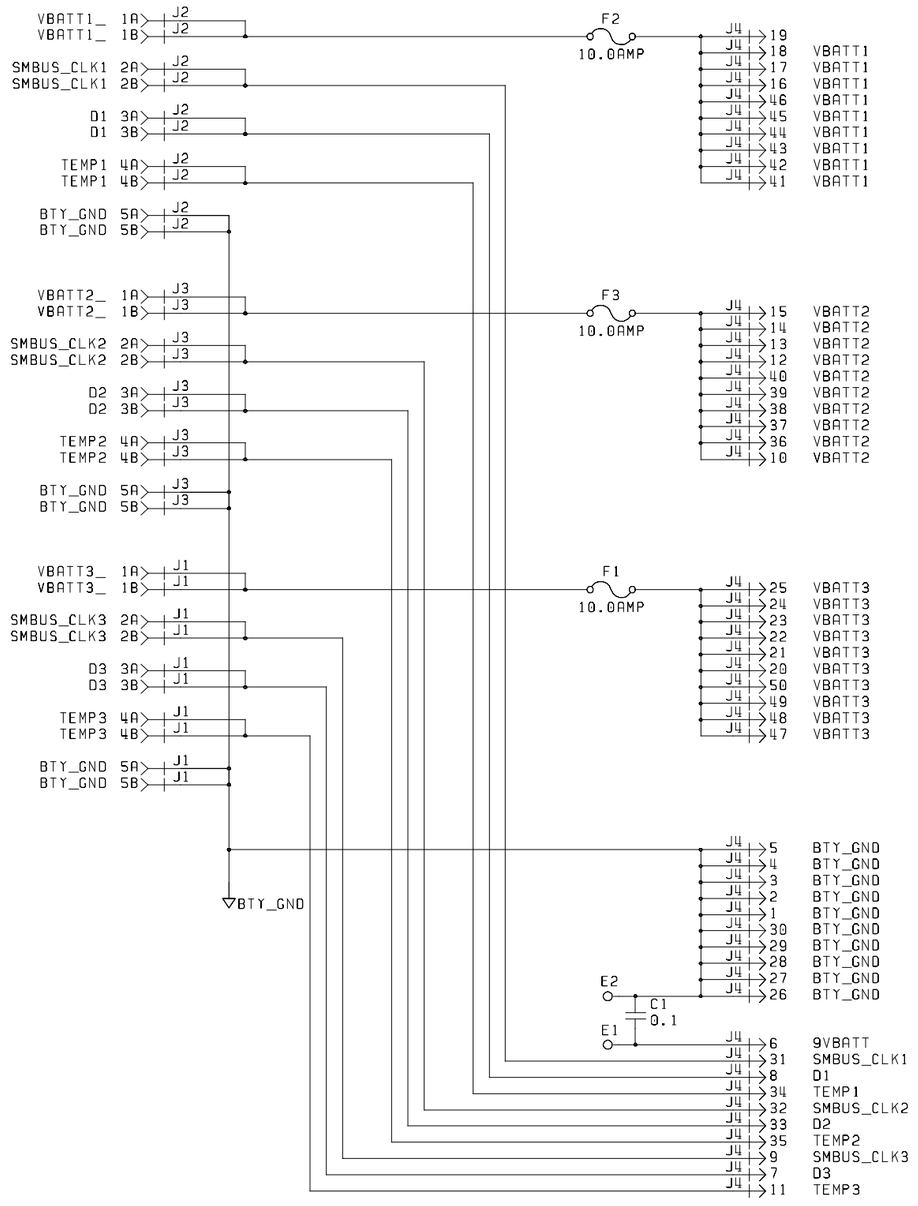


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      J6
   B. REFERENCE DESIGNATORS NOT USED:
      J1-J4

SC313-118 A
Interconnect Flex PWA Schematic

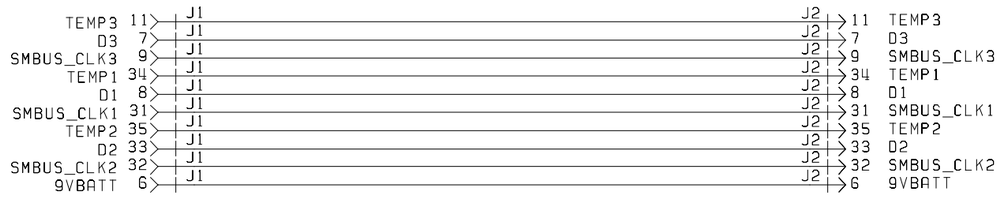


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      J4,F3,C1,E2.
   B. REFERENCE DESIGNATORS NOT USED:
      NONE

SC313-119 A
Battery Flex PWA Schematic



(J1 CONNECTS TO BATTERY FLEX)

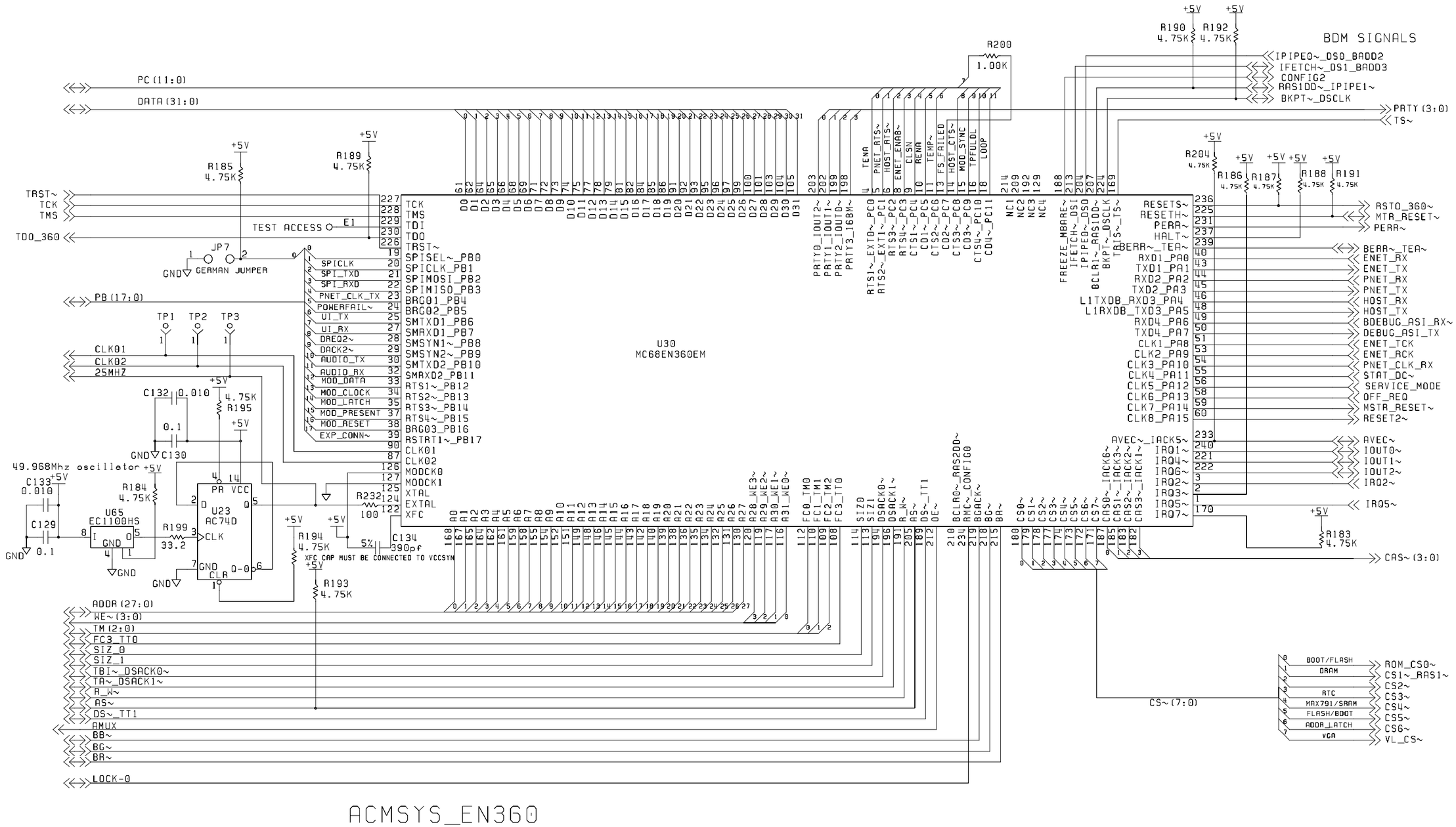
(J2 CONNECTS TO SSSB PWA)

NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

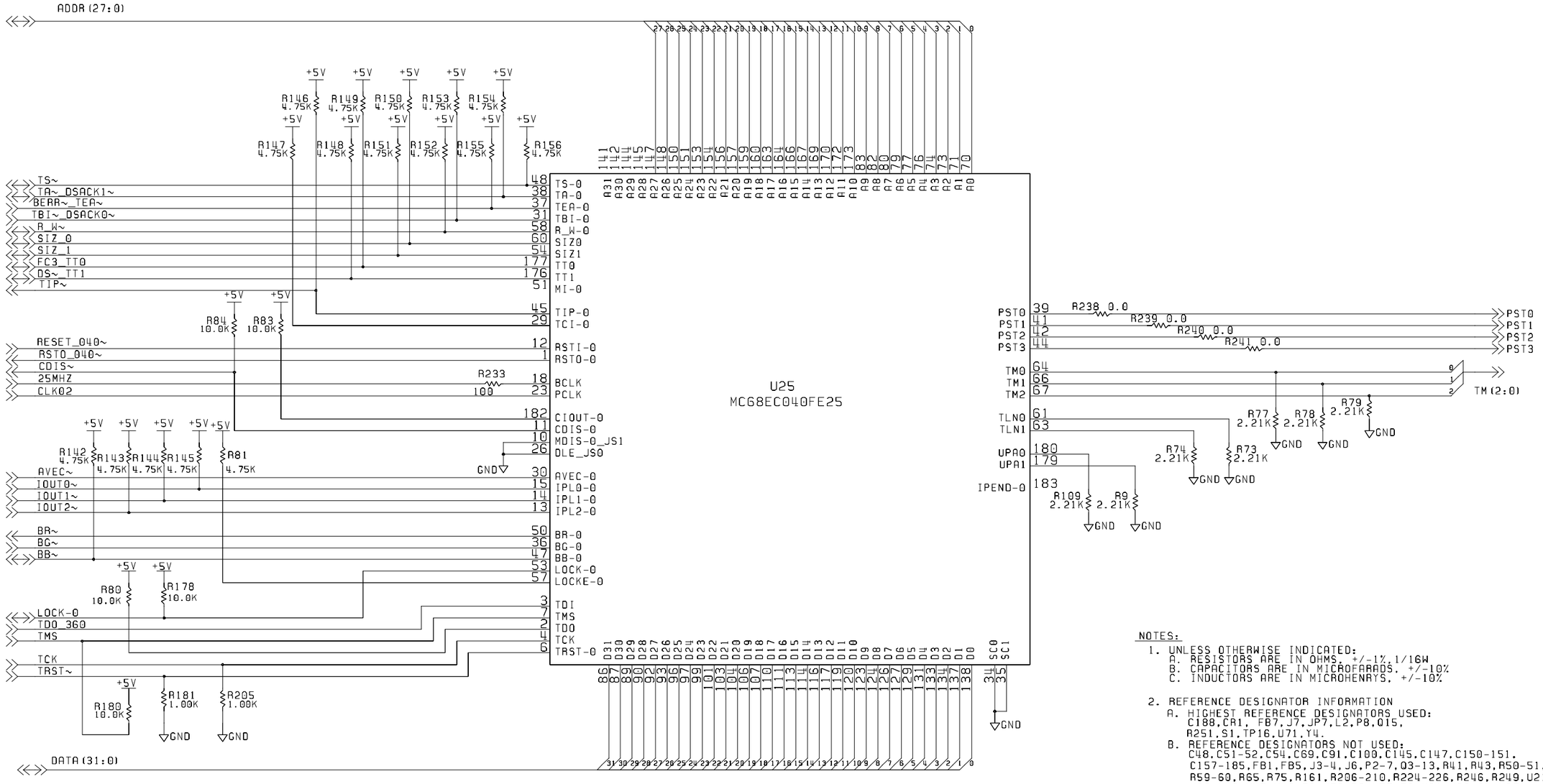
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      J2
   B. REFERENCE DESIGNATORS NOT USED:
      NONE

SC313-120 A
SSB Battery Flex PWA Schematic



ACMSYS_EN360

SC315-522 C
System Processor PWA Schematic (1 of 17)



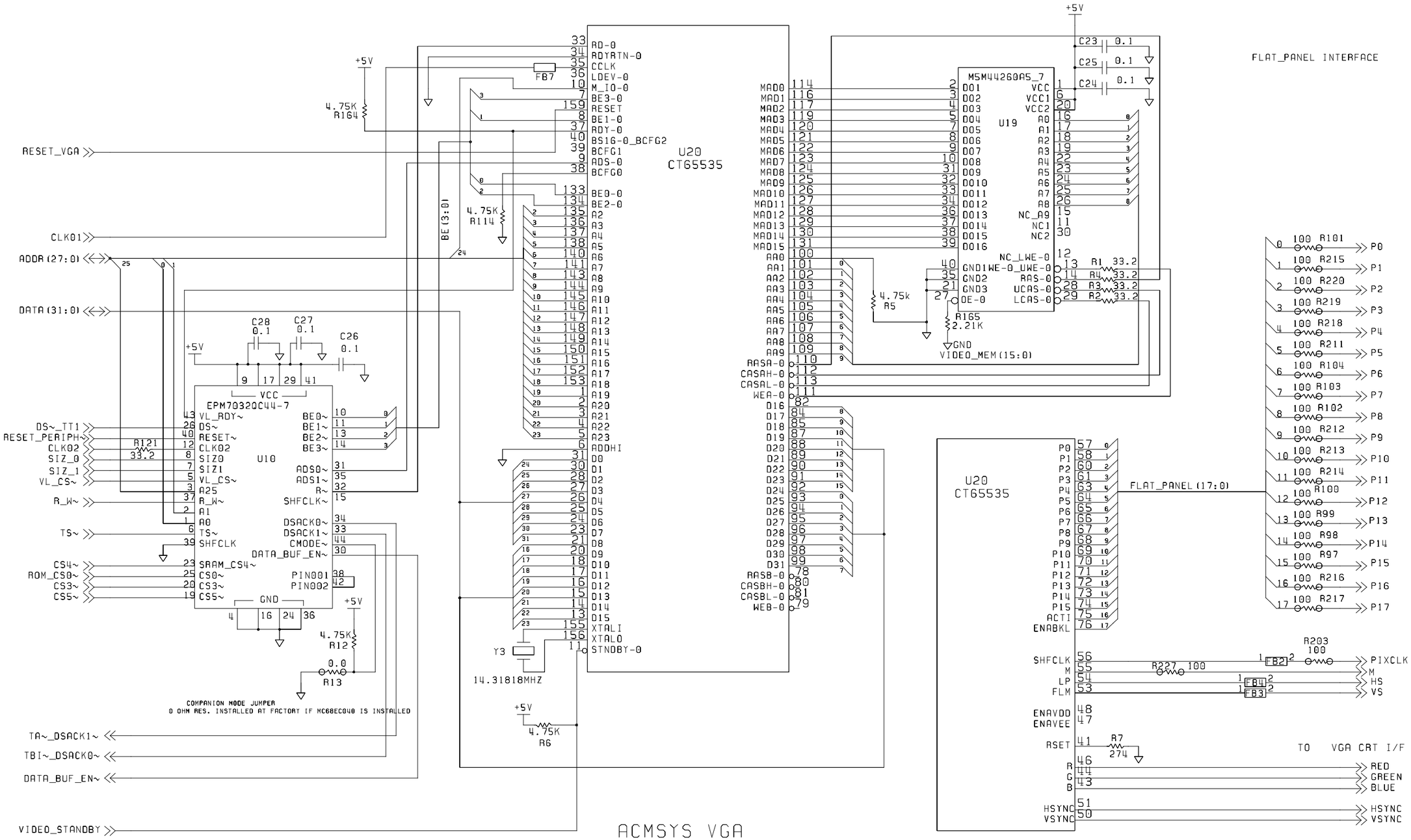
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/16W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

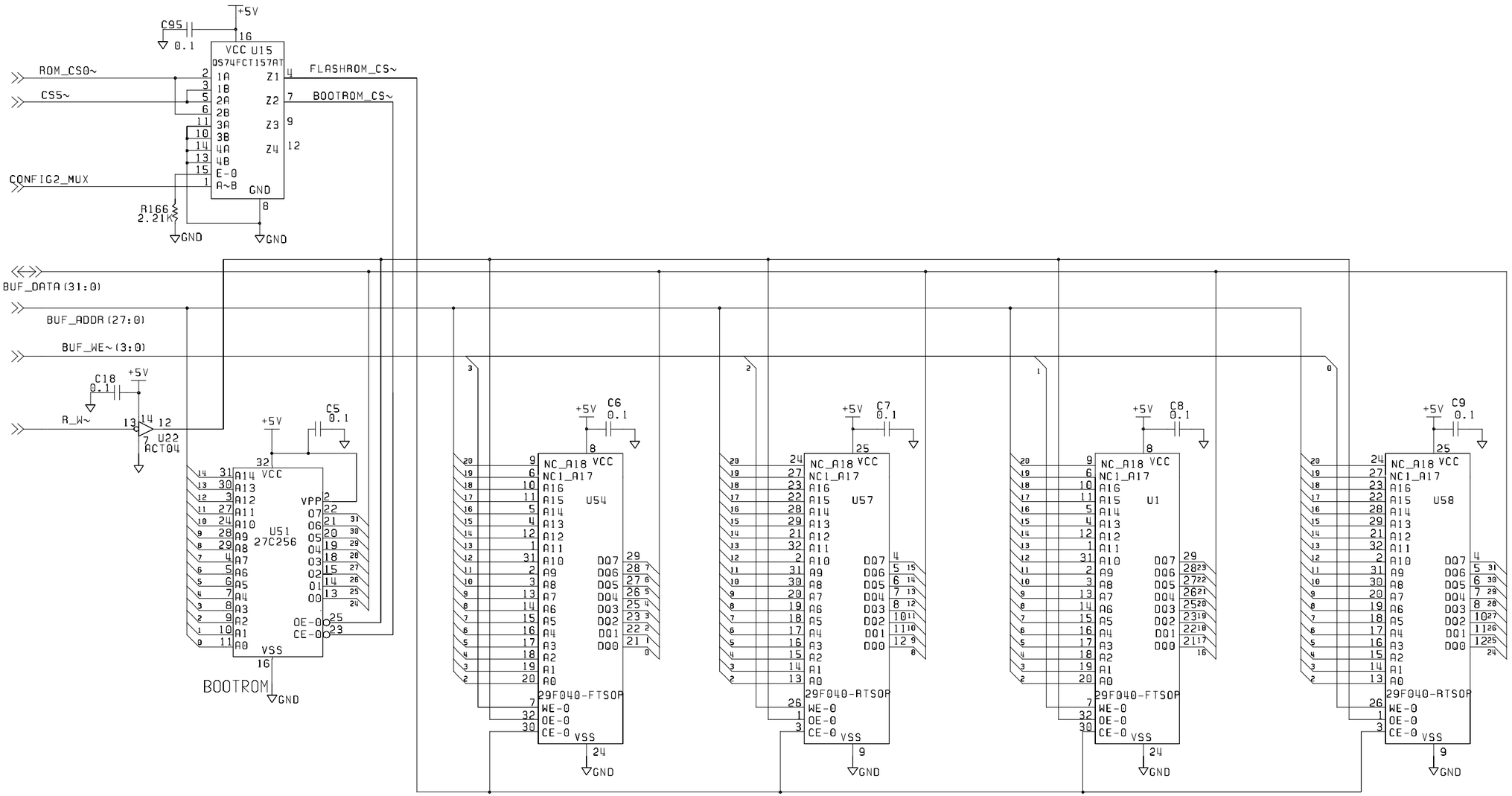
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C188,CR1, FB7,J7,JP7,L2,P8,Q15,
      R251,S1,TP16,U71,Y4.
   B. REFERENCE DESIGNATORS NOT USED:
      C48,C51-52,C54,C69,C91,C100,C145,C147,C150-151,
      C157-185,FB1,FB5,J3-4,J6,P2-7,Q3-13,R41,R43,R50-51,
      R59-60,R65,R75,R161,R206-210,R224-226,R246,R249,U21,
      U28,U42,U45,U48-50,U52-53,U55-56,U61,U63-64,U67.

ACMSYS EC040

SC315-522 C
System Processor PWA Schematic (2 of 17)

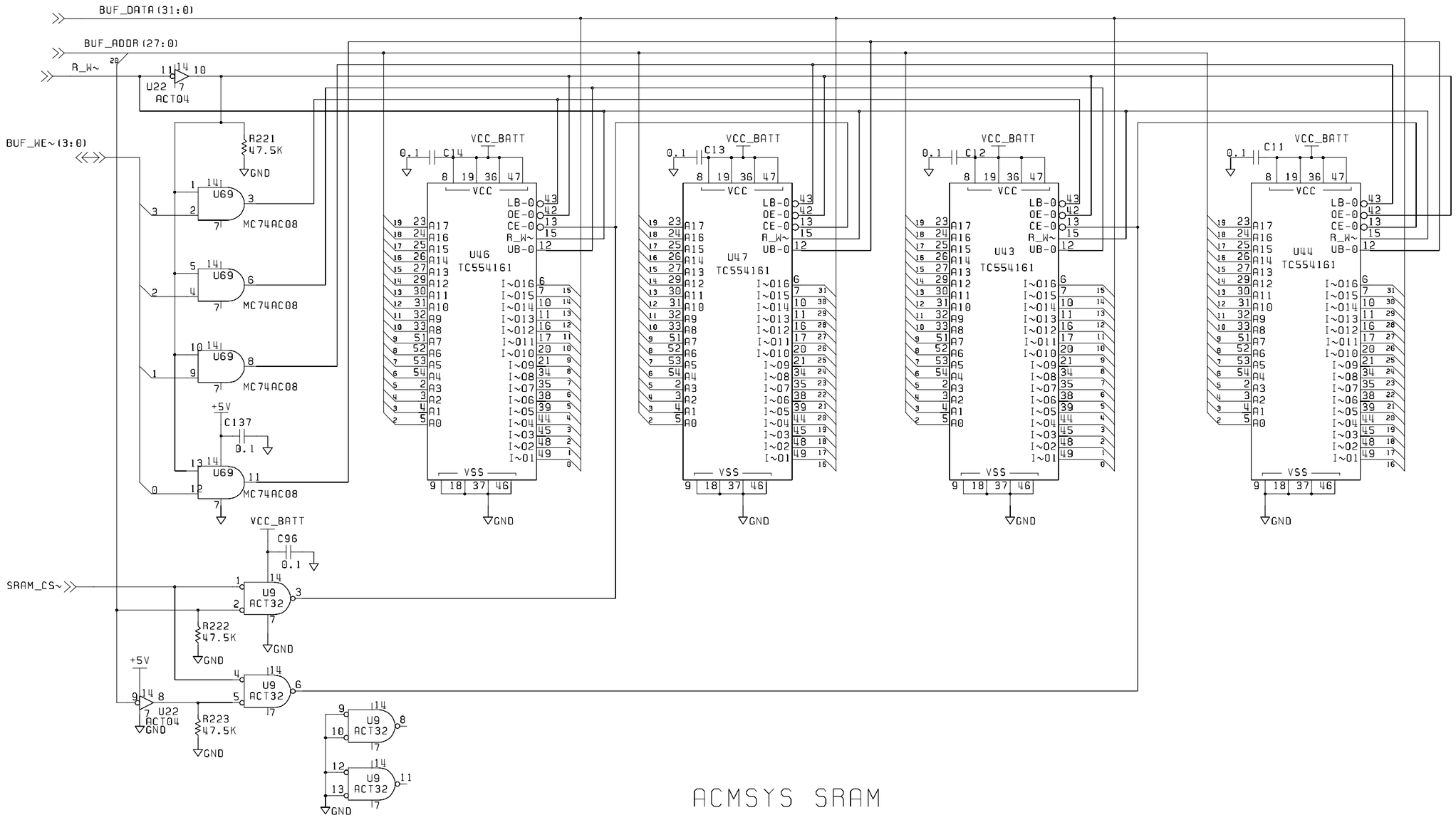


SC315-522 C
System Processor PWA Schematic (3 of 17)



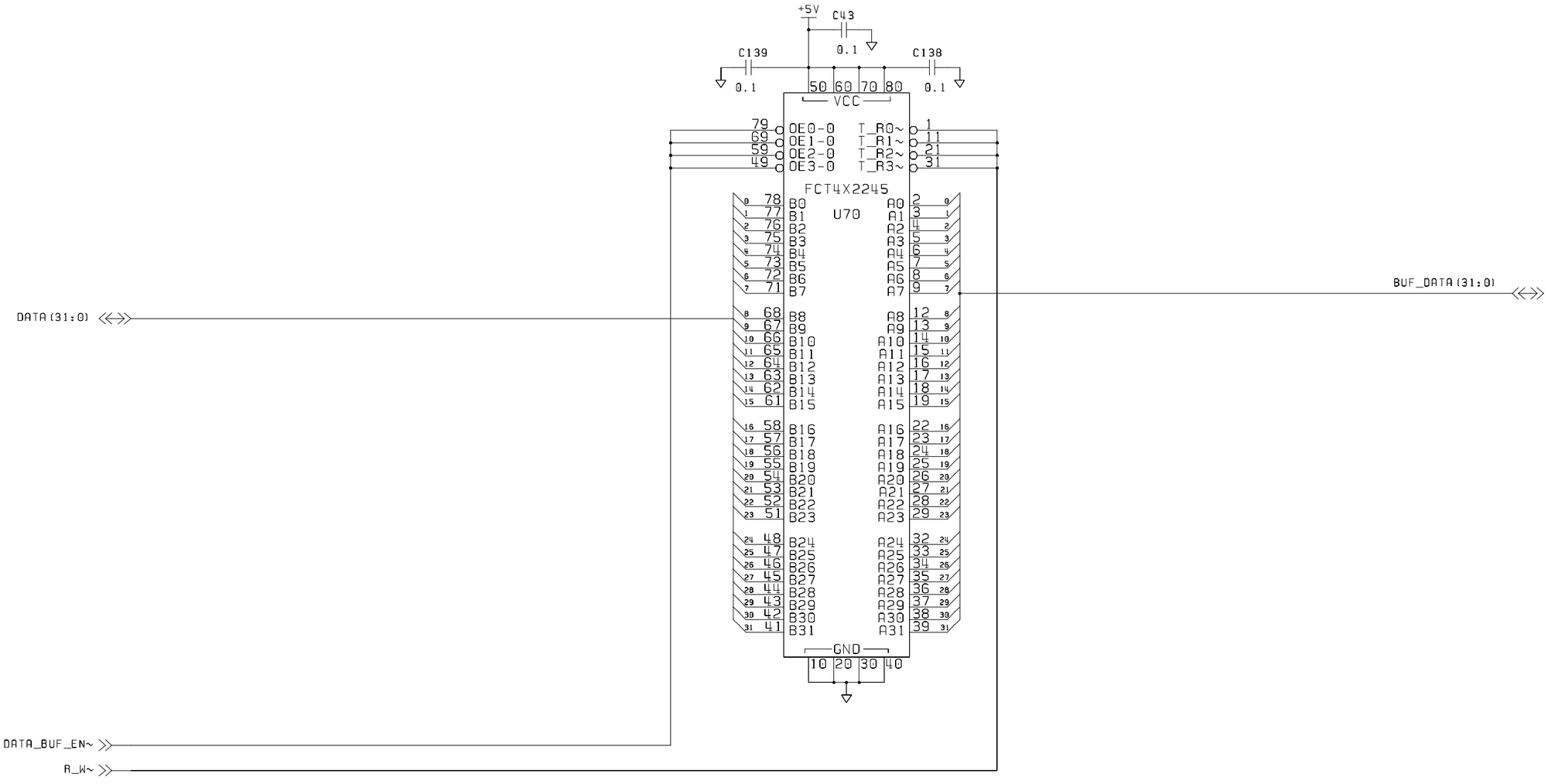
ACMSYS FLASH/BOOTROM

SC315-522 C
System Processor PWA Schematic (4 of 17)



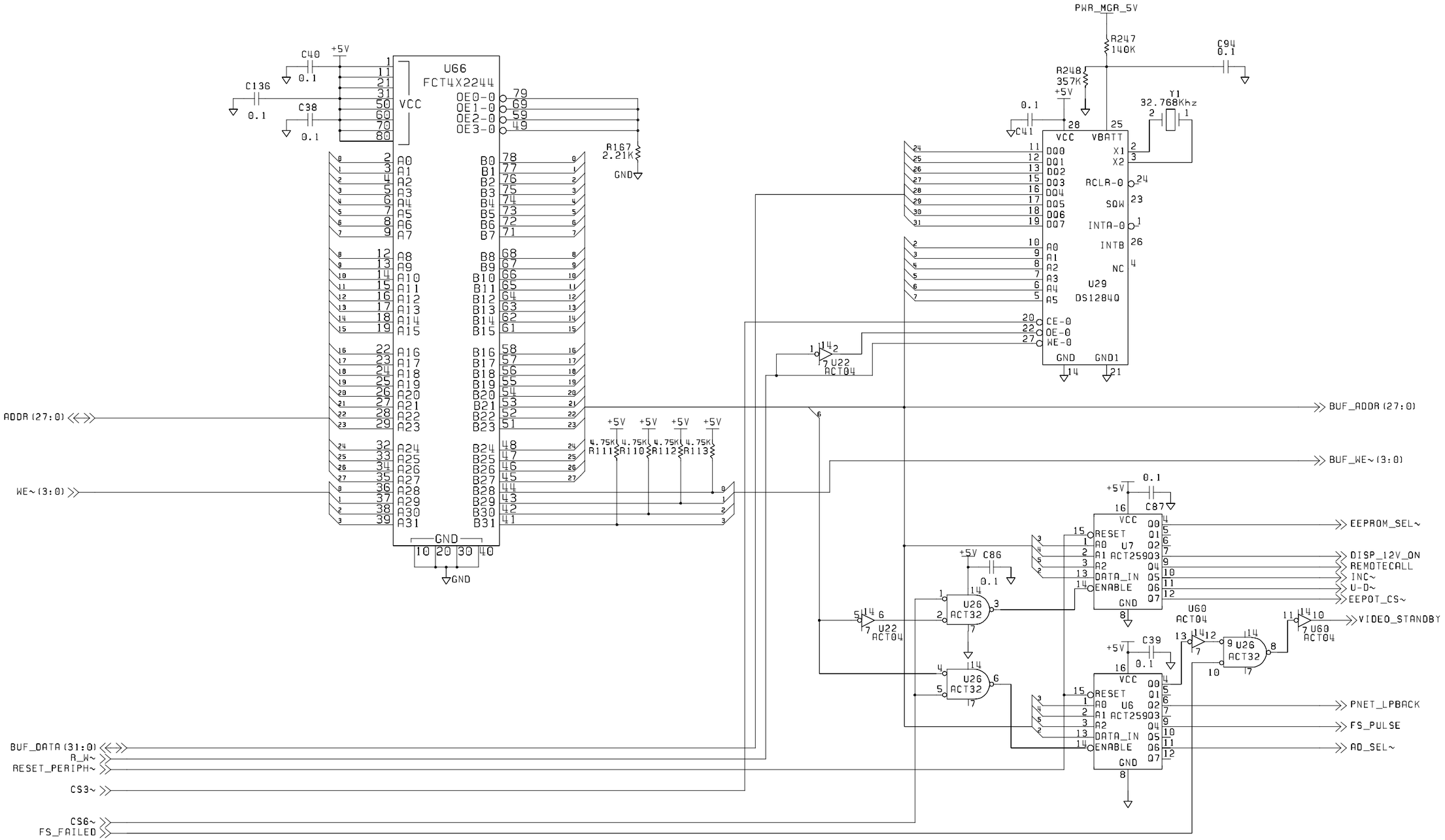
ACMSYS SRAM

SC315-522 C
System Processor PWA Schematic (5 of 17)



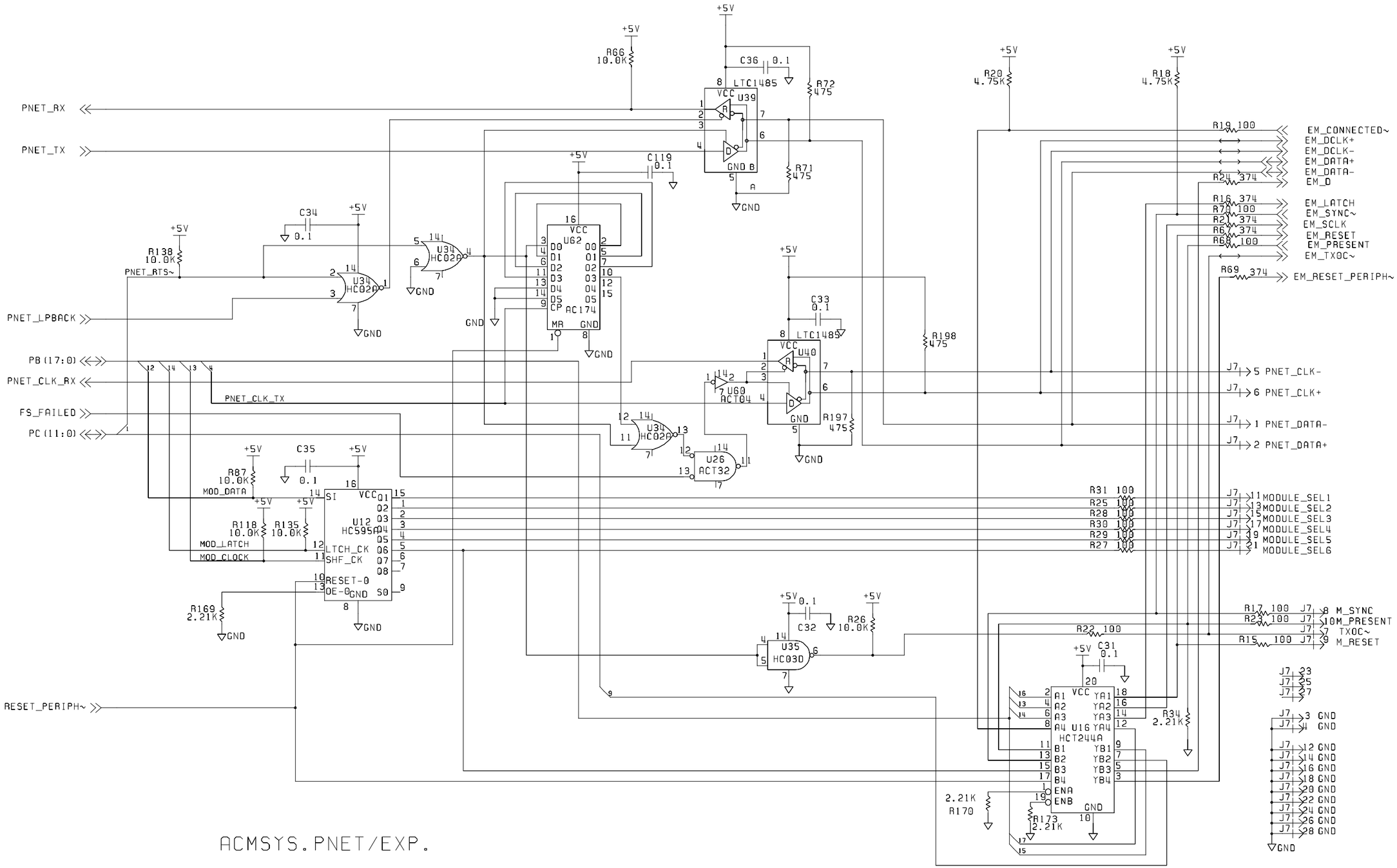
ACMSYS DATA BUFFERS

SC315-522 C
System Processor PWA Schematic (6 of 17)

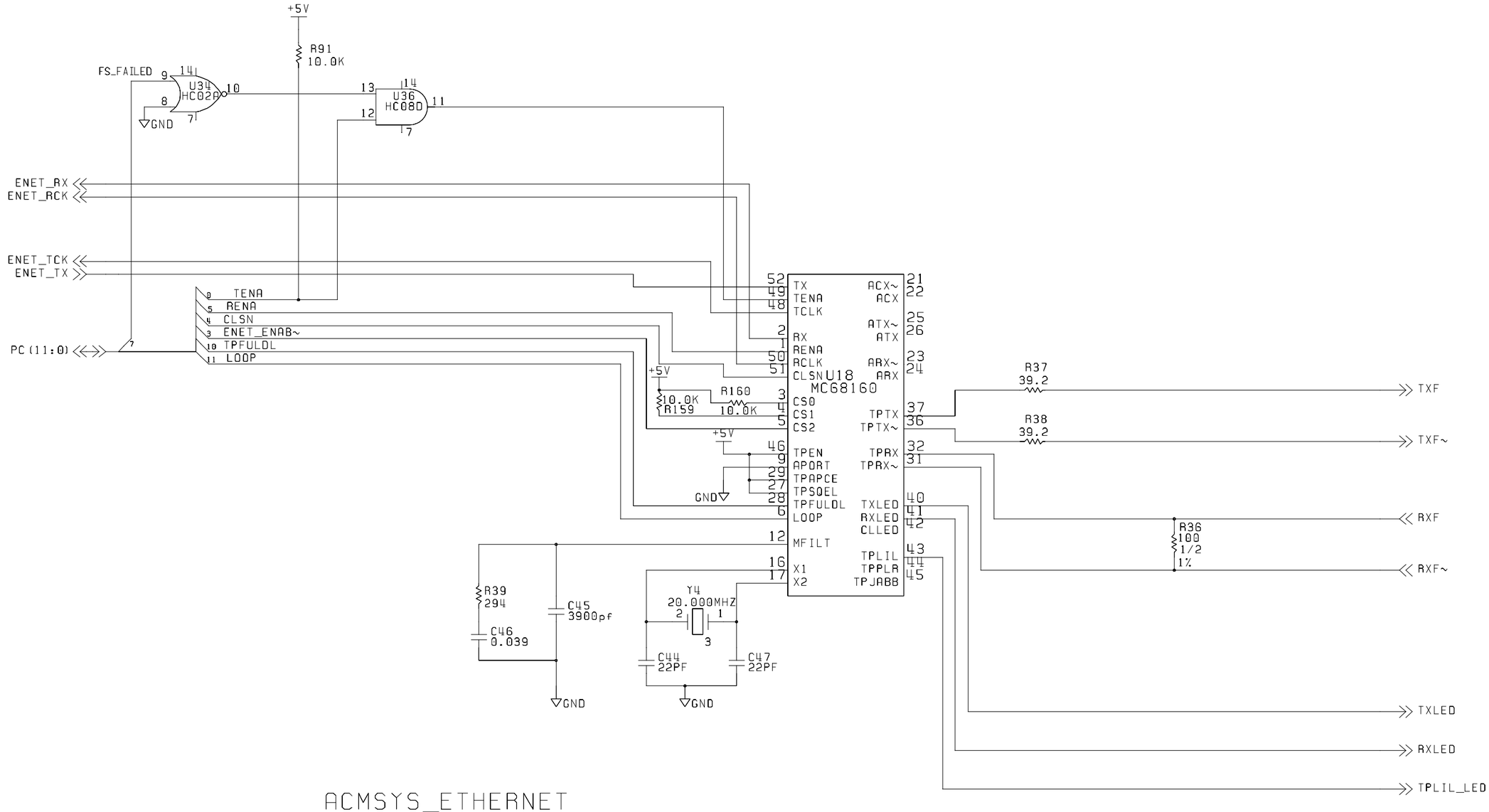


ACMSYS ADDR BUF/RTC

SC315-522 C
System Processor PWA Schematic (7 of 17)

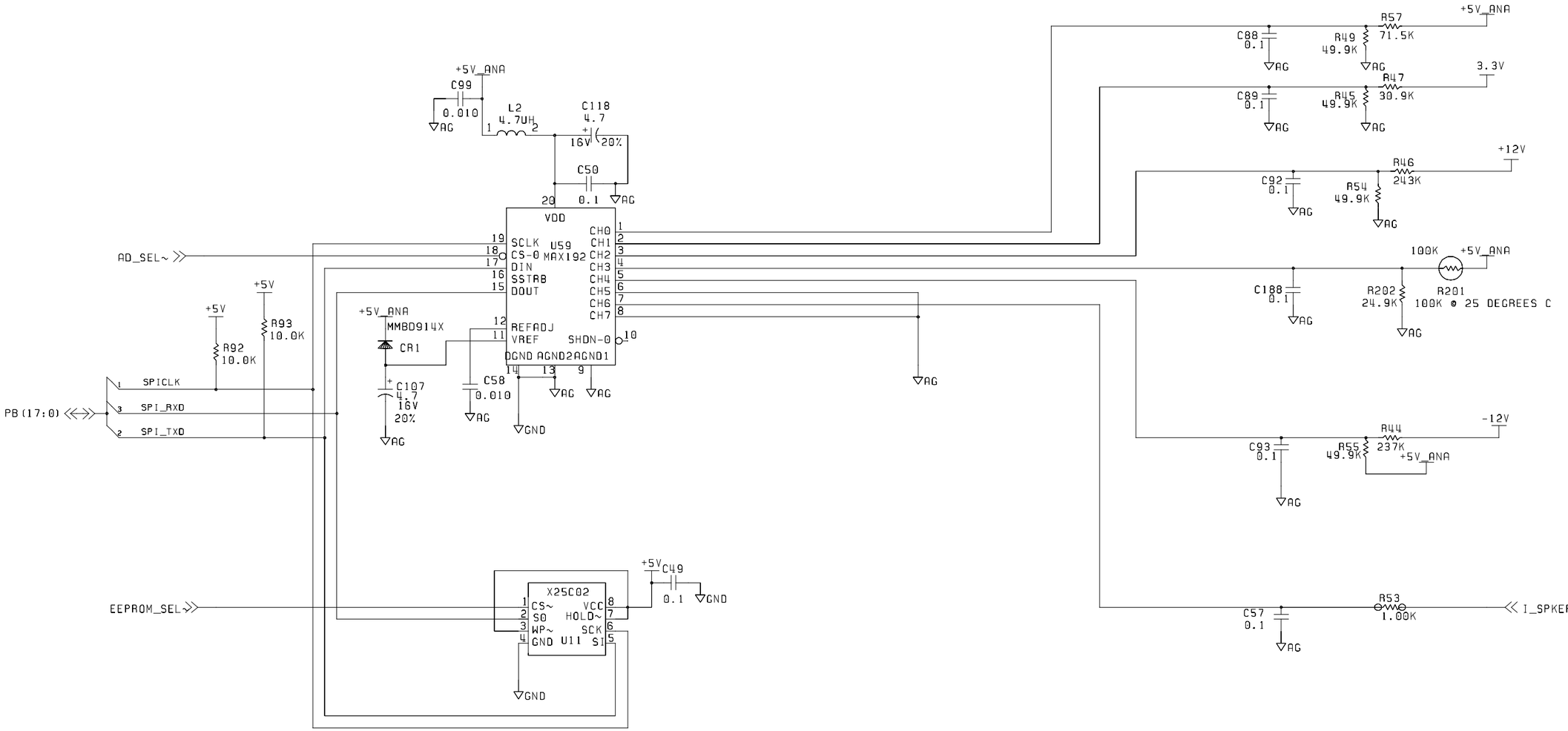


SC315-522 C
System Processor PWA Schematic (8 of 17)



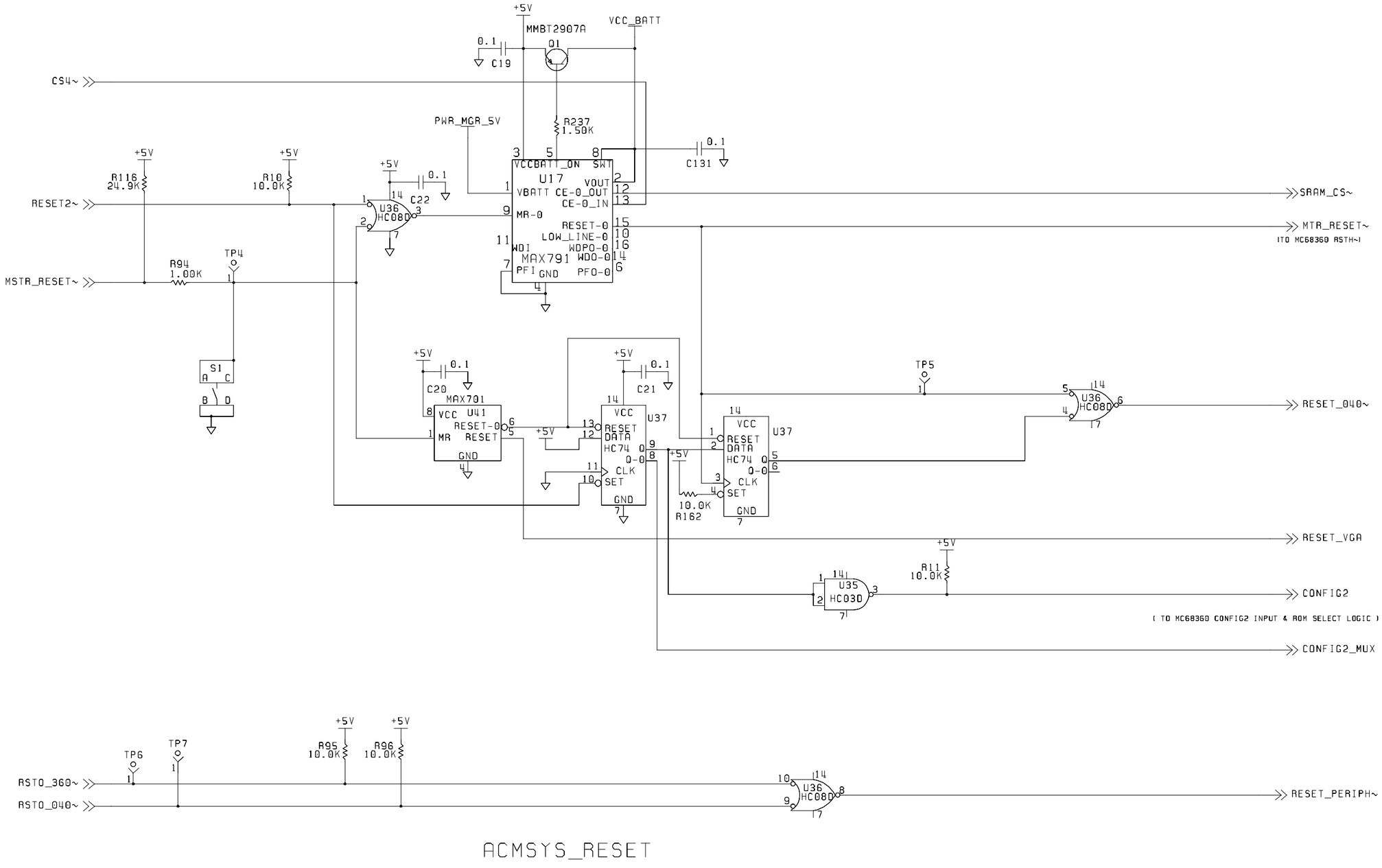
ACMSYS_ETHERNET

SC315-522 C
System Processor PWA Schematic (9 of 17)



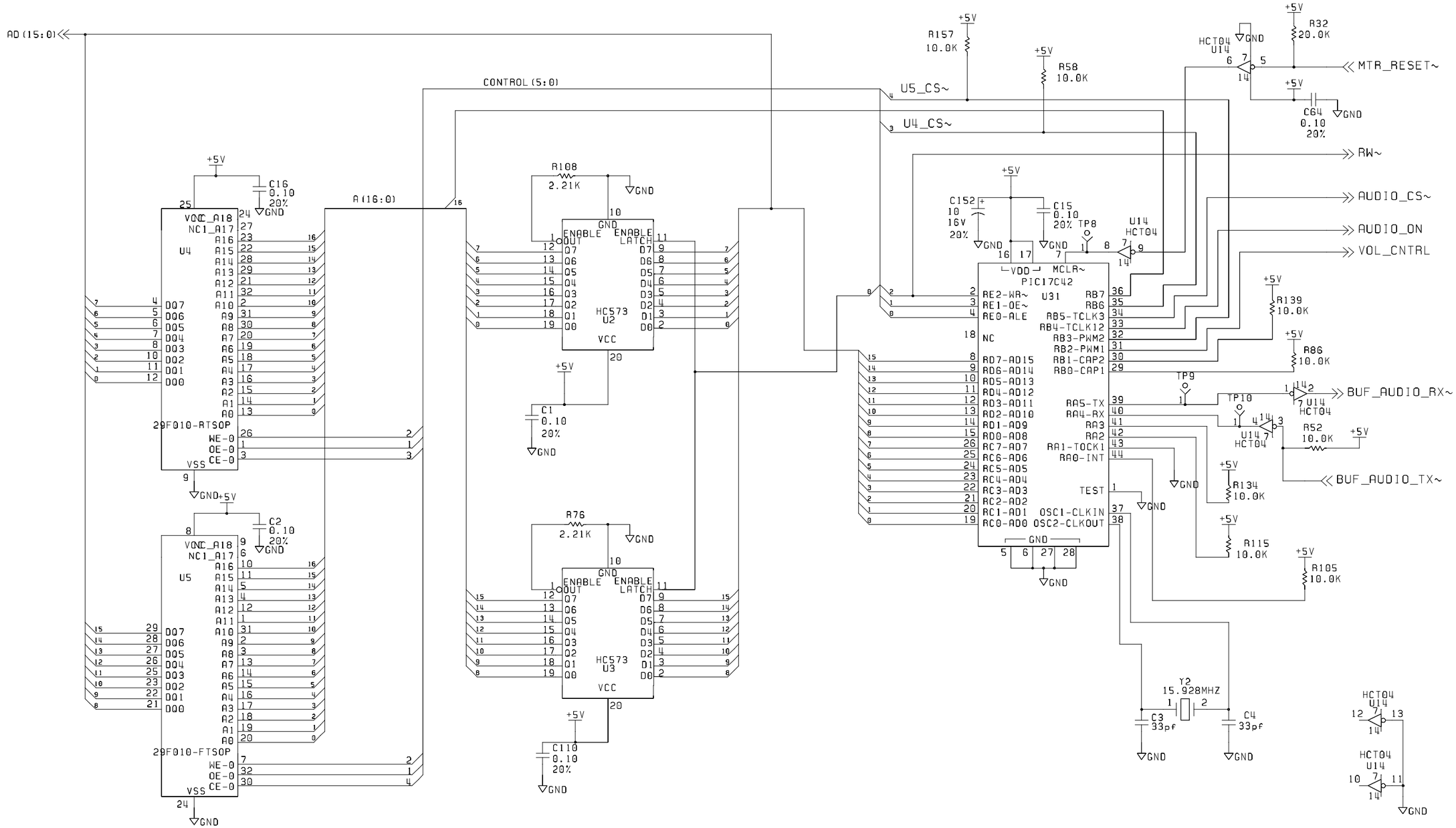
ACMSYS_SPI

SC315-522 C
System Processor PWA Schematic (10 of 17)

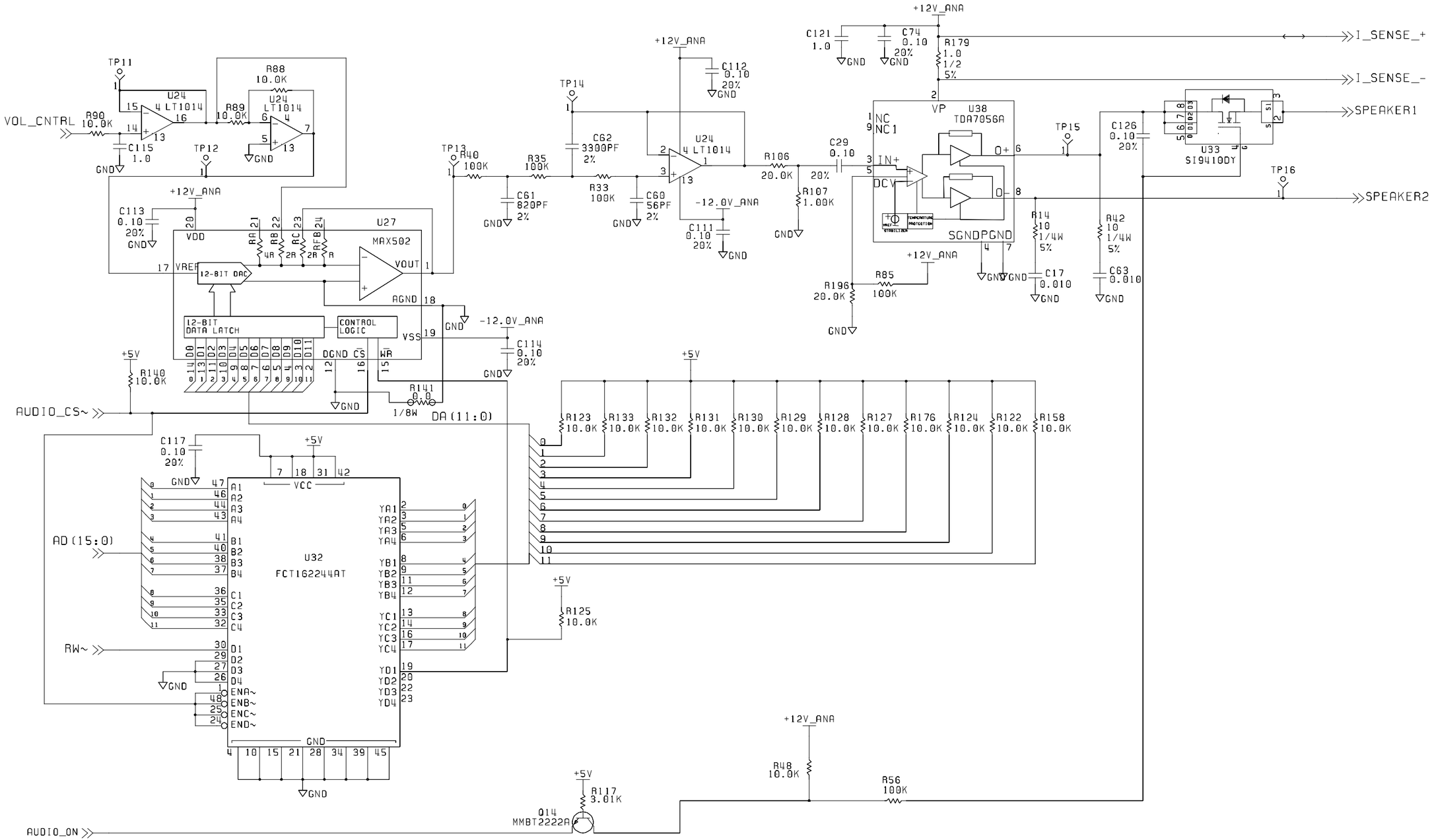


ACMSYS_RESET

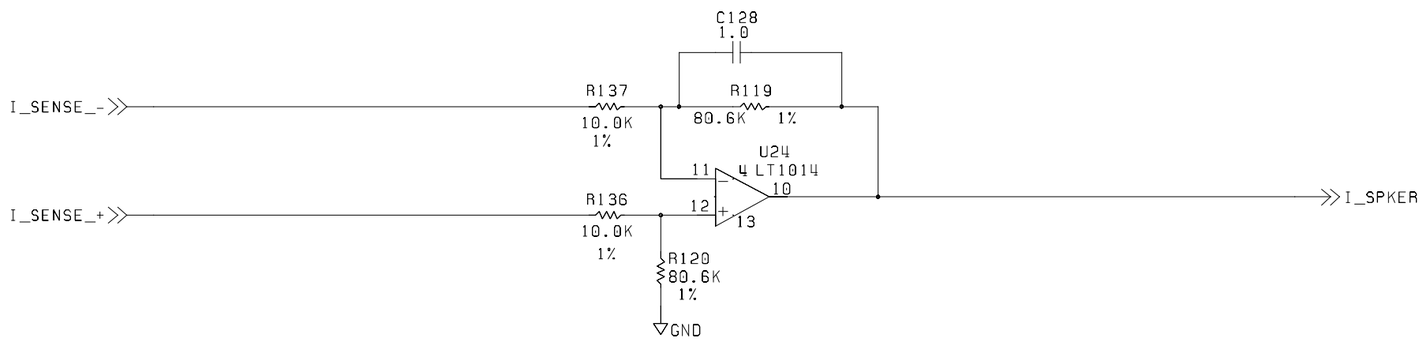
SC315-522 C
System Processor PWA Schematic (11 of 17)

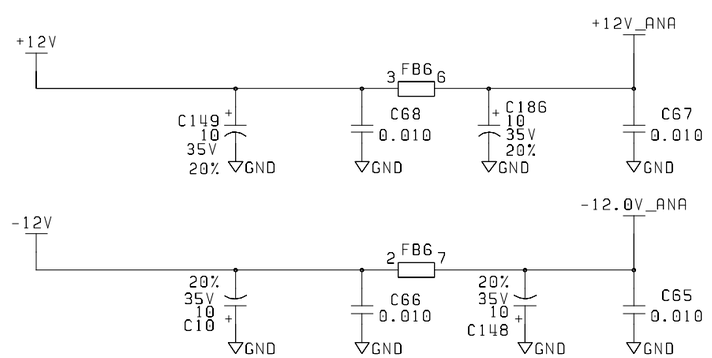


SC315-522 C
System Processor PWA Schematic (12 of 17)

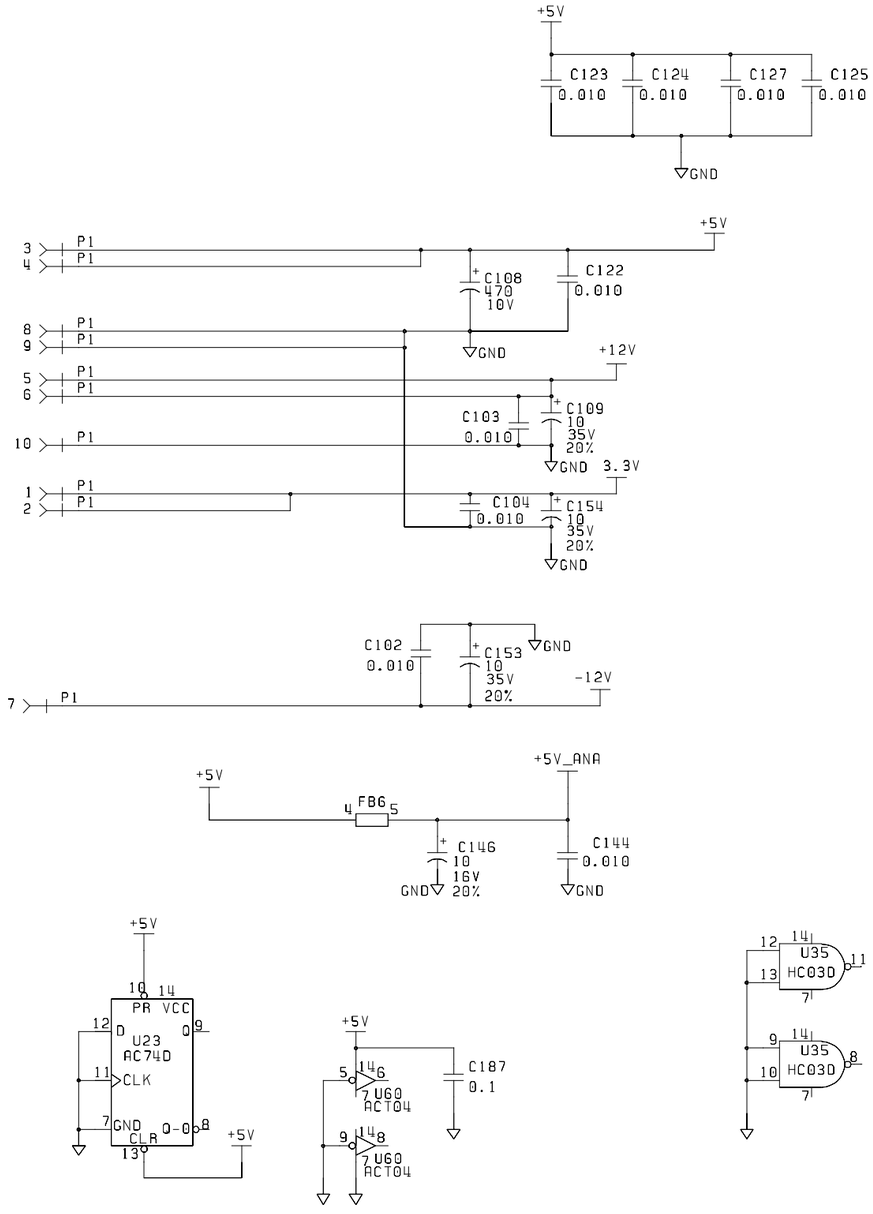


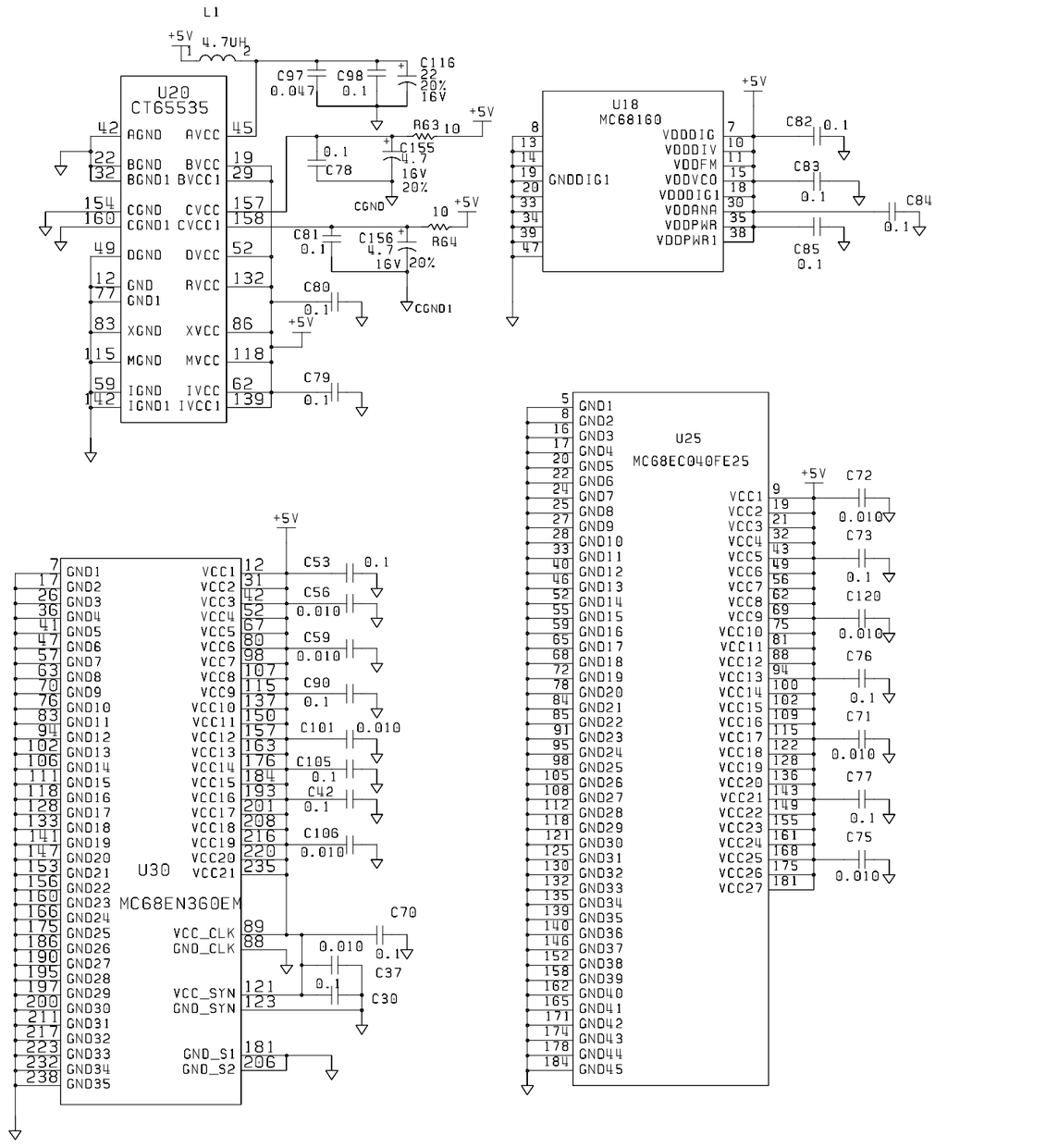
SC315-522 C
System Processor PWA Schematic (13 of 17)



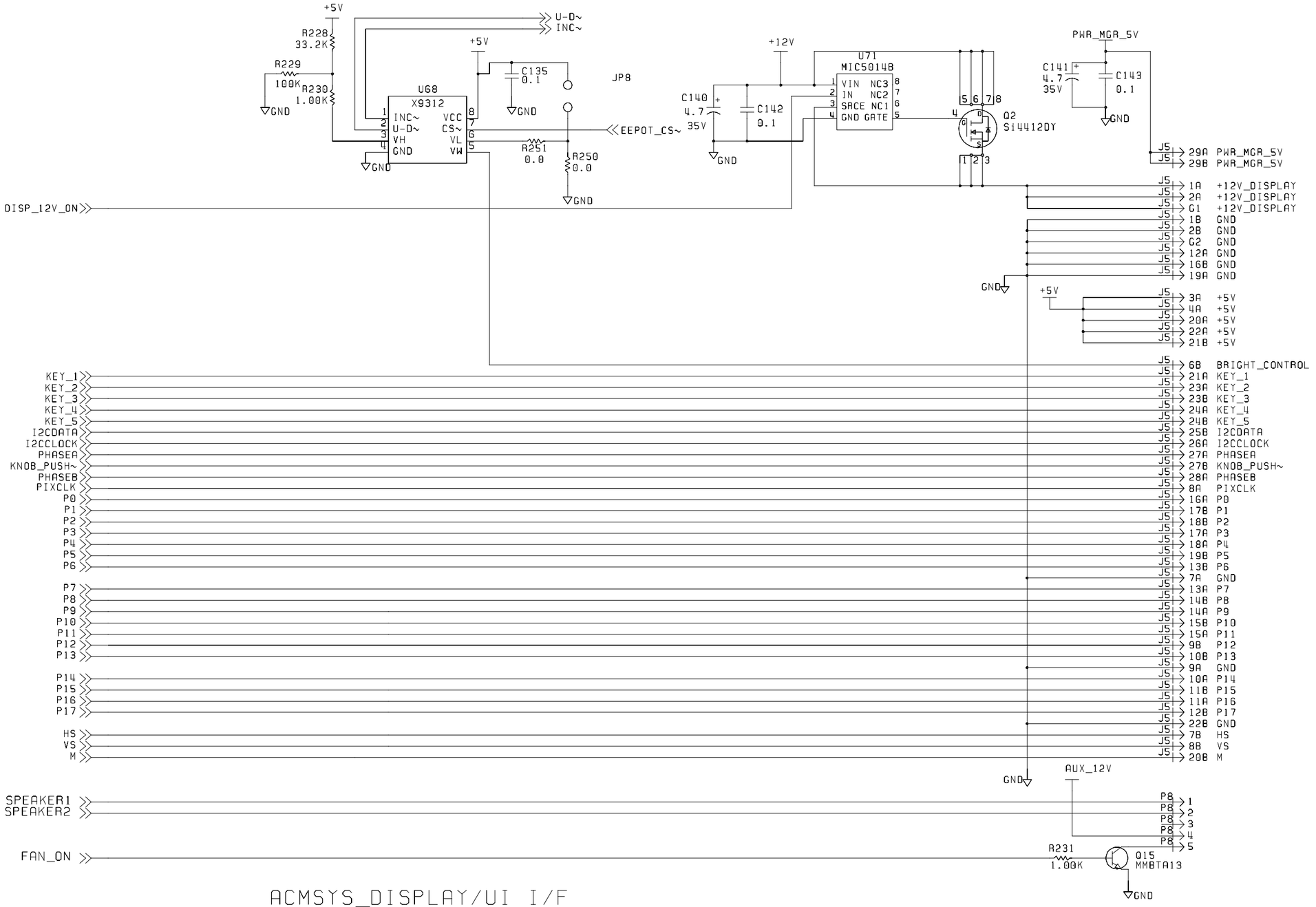


SC315-522 C
System Processor PWA Schematic (14 of 17)

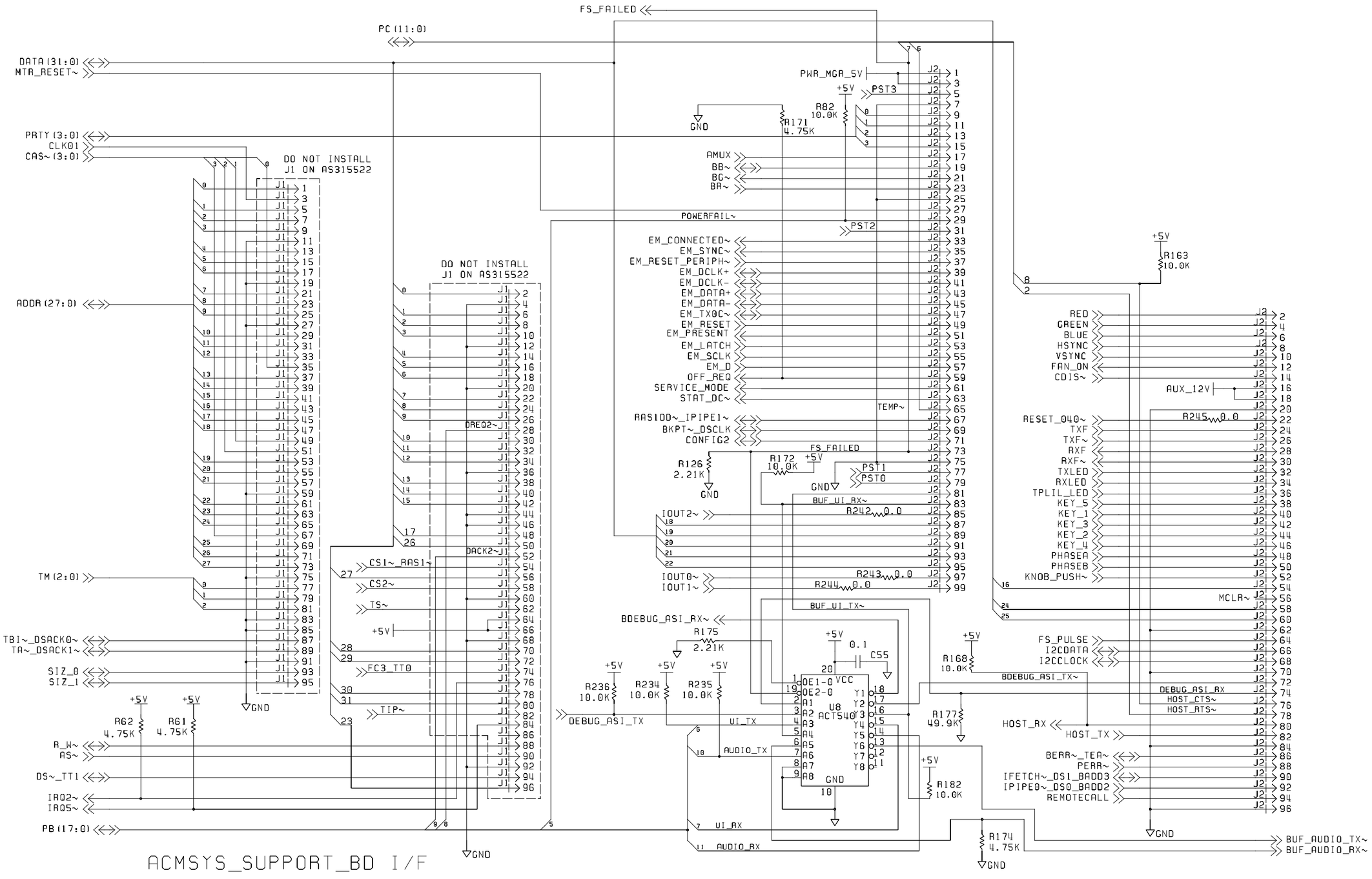




SC315-522 C
System Processor PWA Schematic (15 of 17)

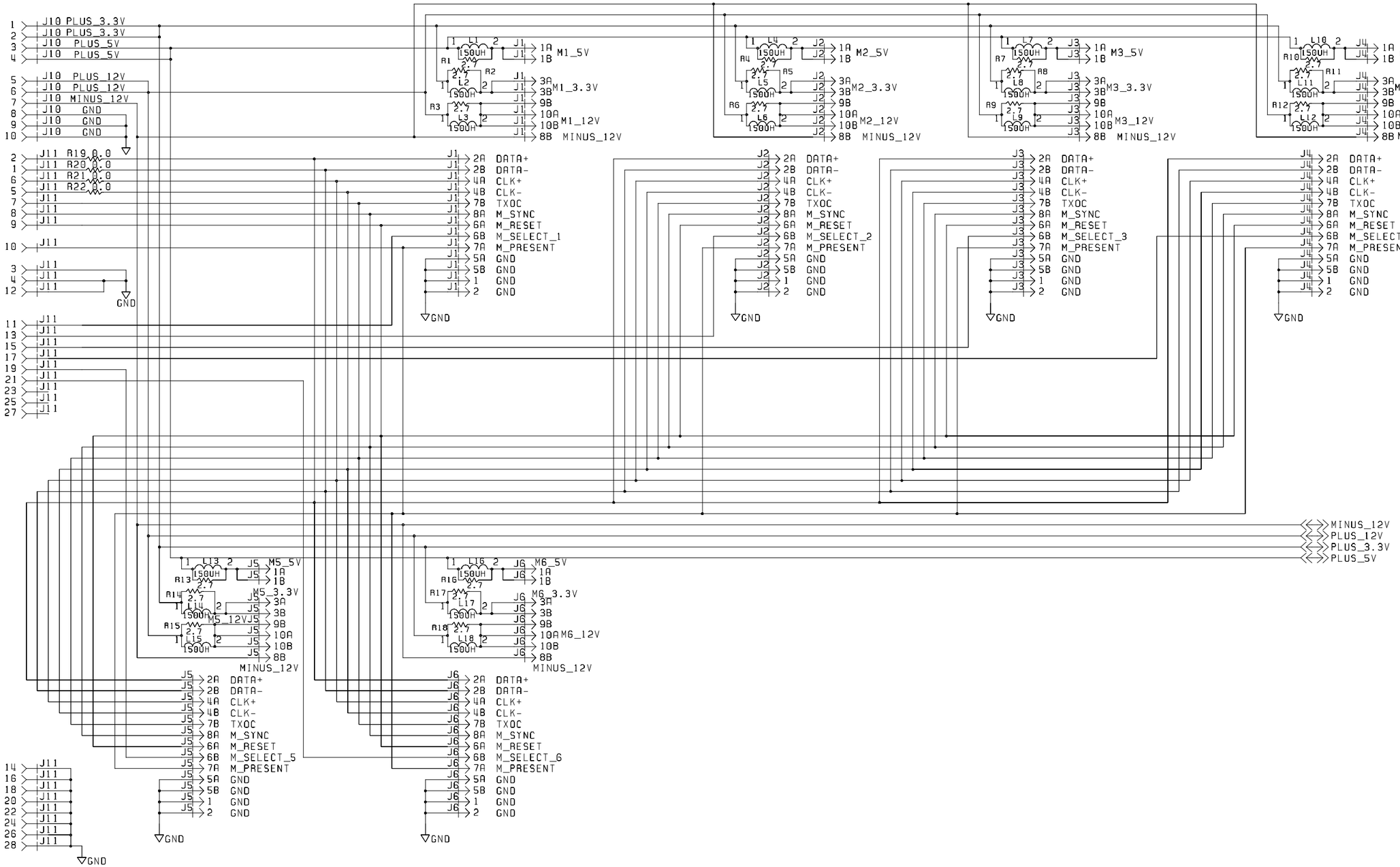


SC315-522 C
System Processor PWA Schematic (16 of 17)

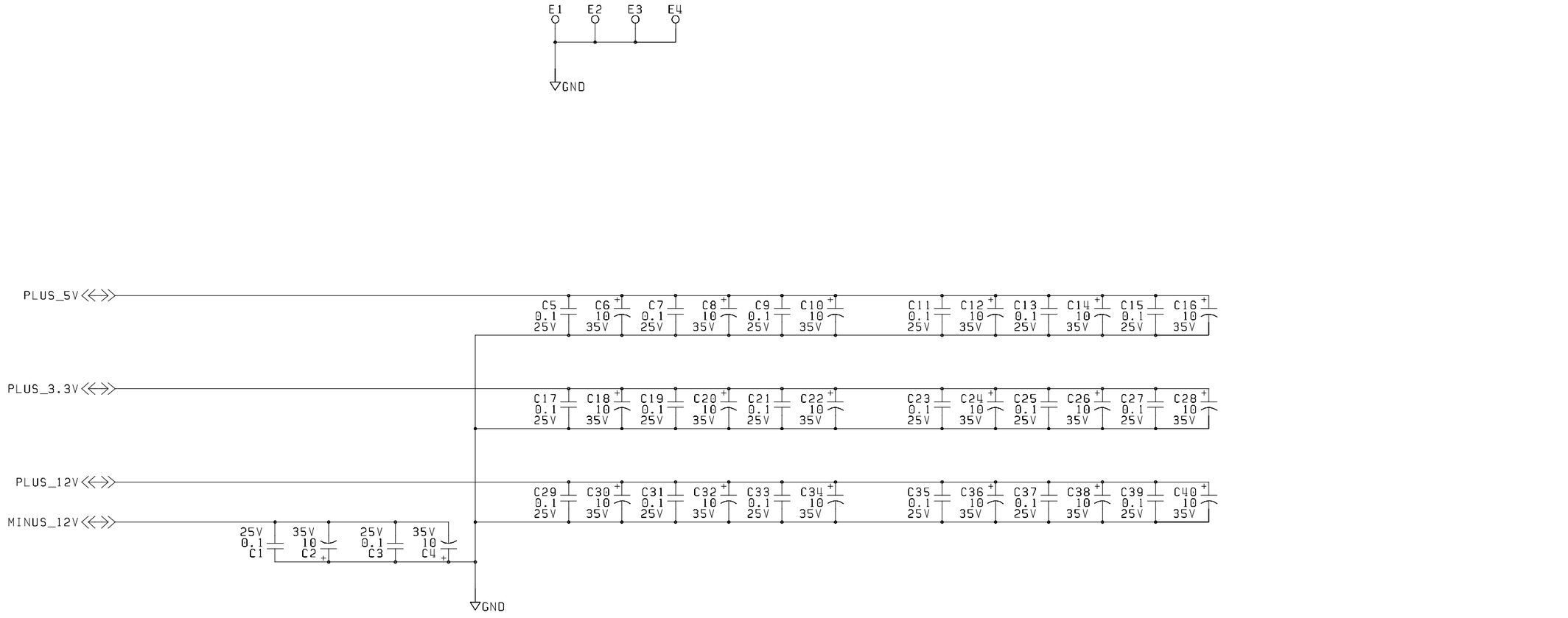


ACMSYS_SUPPORT_BD I/F

SC315-522 C
System Processor PWA Schematic (17 of 17)



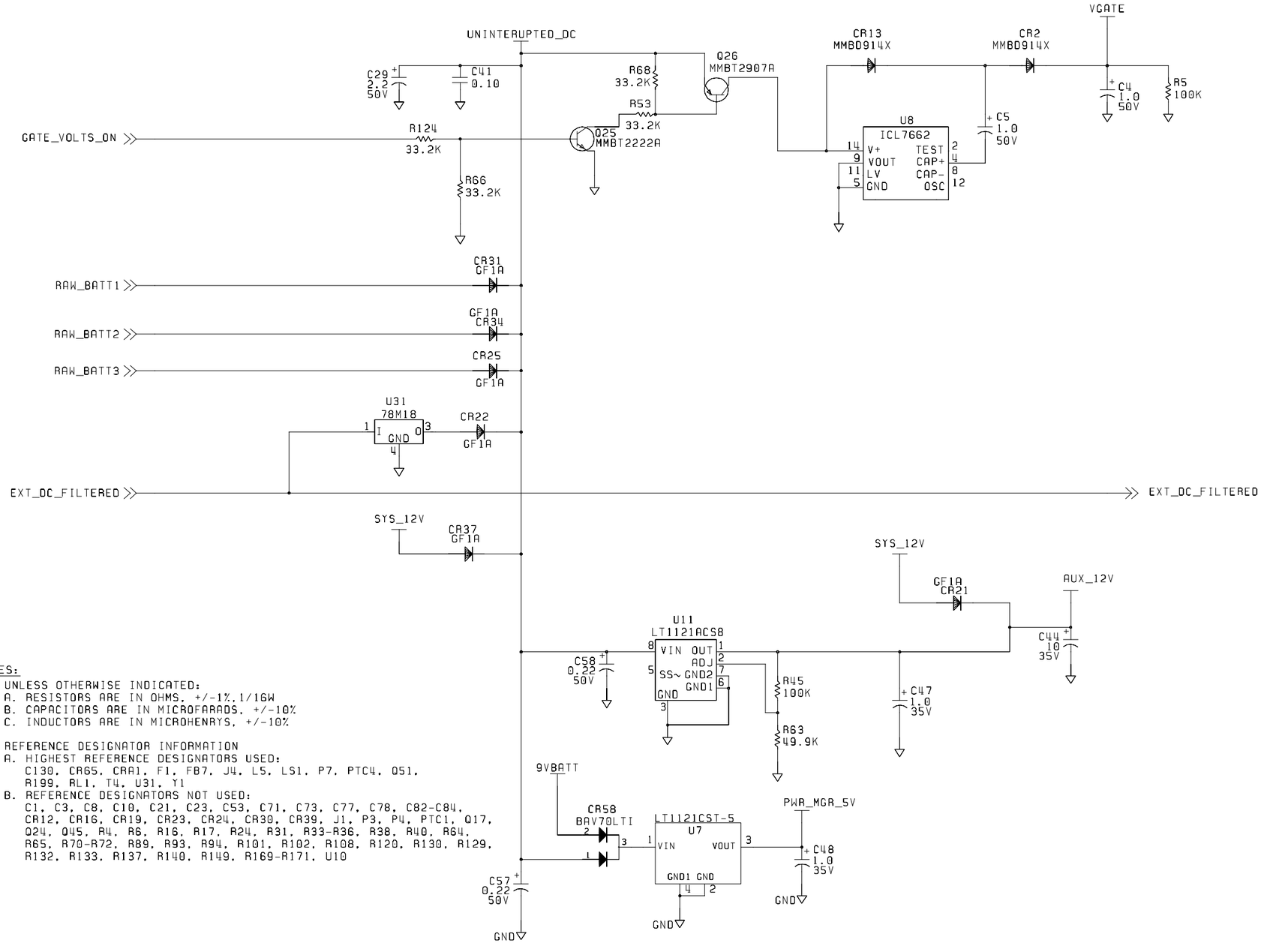
SC315-523 A
Backplane PWA Schematic (1 of 2)



NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-5%,1/8W
   B. CAPACITORS ARE IN MICROFARADS.
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED: C40, J11, L18, R22
   B. REFERENCE DESIGNATORS NOT USED: J7-J9

SC315-523 A
Backplane PWA Schematic (2 of 2)

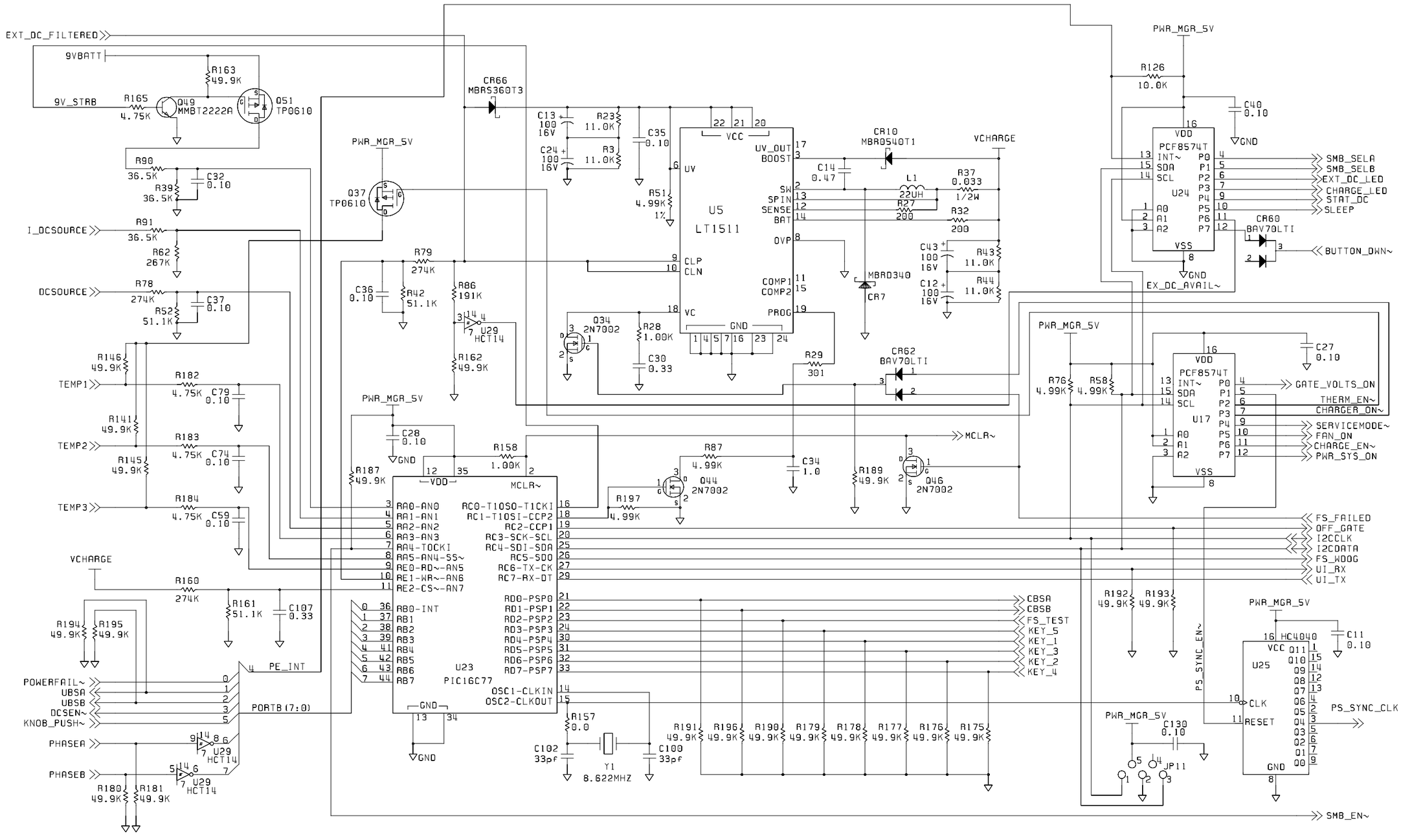


NOTES:

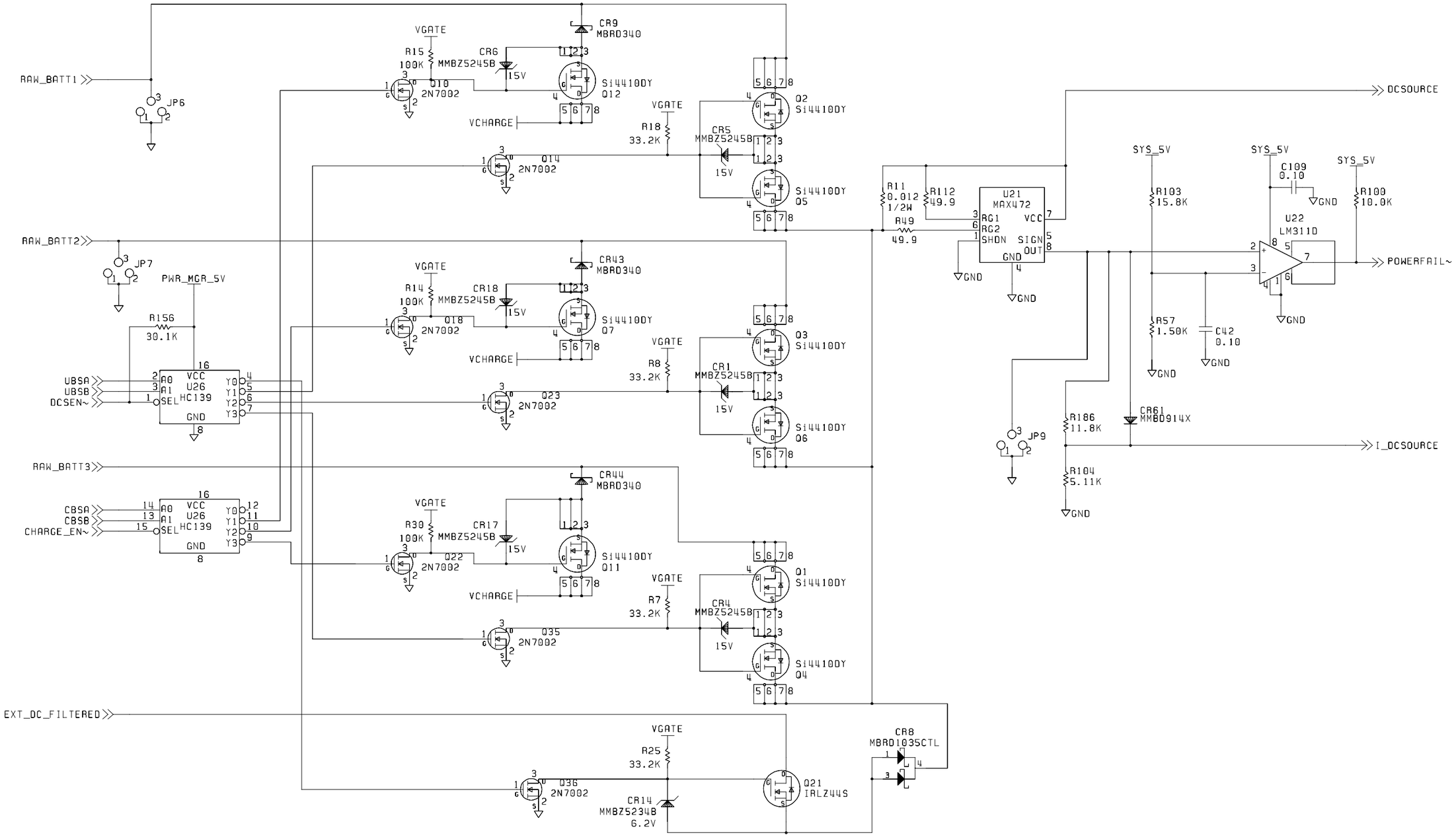
1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/16W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C130, CR65, CRA1, F1, FB7, J4, L5, LS1, P7, PTC4, Q51,
      R199, RL1, T4, U31, Y1
   B. REFERENCE DESIGNATORS NOT USED:
      C1, C3, C8, C10, C21, C23, C53, C71, C73, C77, C78, C82-C84,
      CR12, CR16, CR19, CR23, CR24, CR30, CR39, J1, P3, P4, PTC1, Q17,
      Q24, Q45, R4, R6, R16, R17, R24, R31, R33-R36, R38, R40, R64,
      R65, R70-R72, R89, R93, R94, R101, R102, R108, R120, R130, R129,
      R132, R133, R137, R140, R149, R169-R171, U10

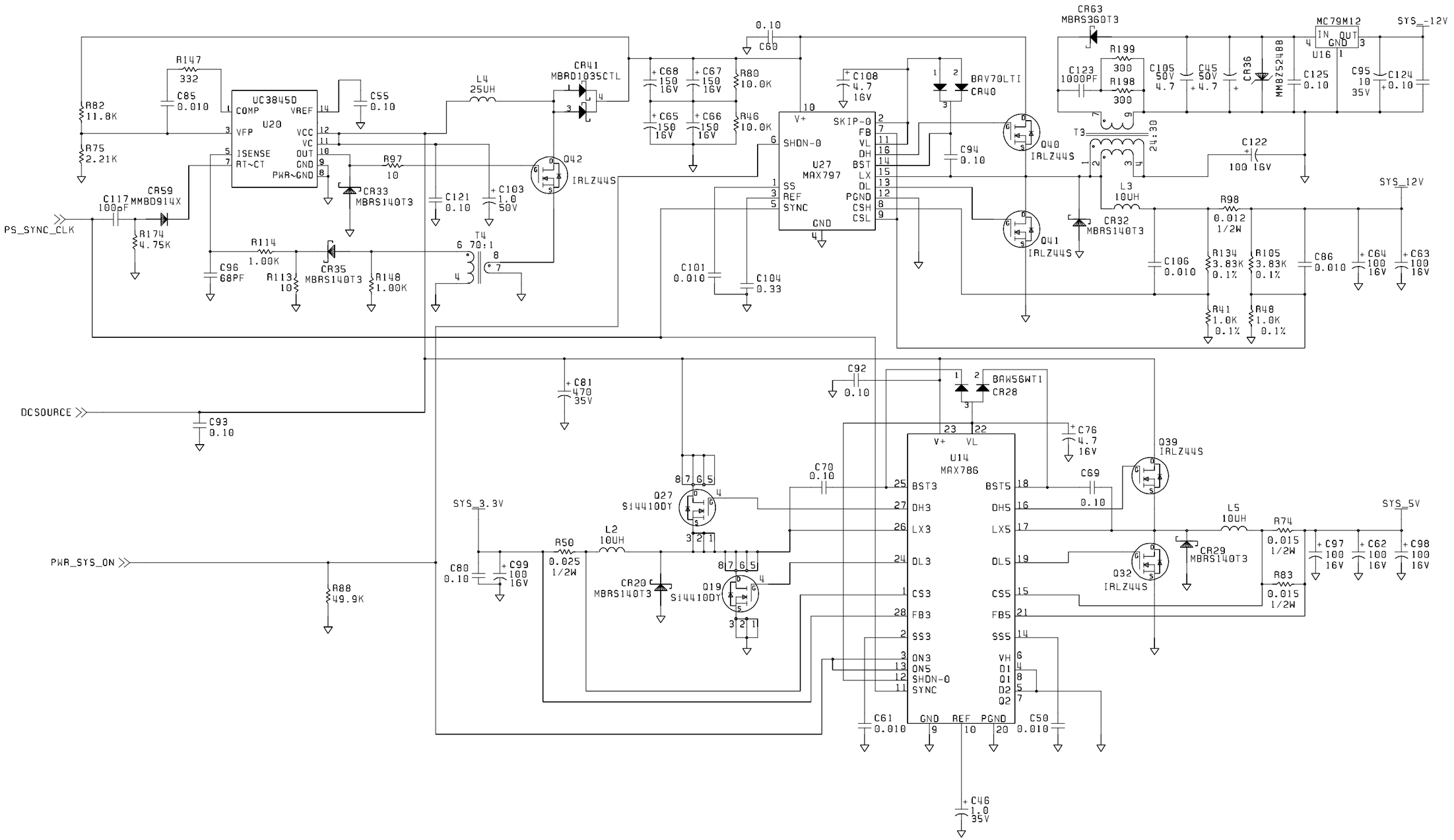
SC315-524 B
System Support PWA Schematic (1 of 11)



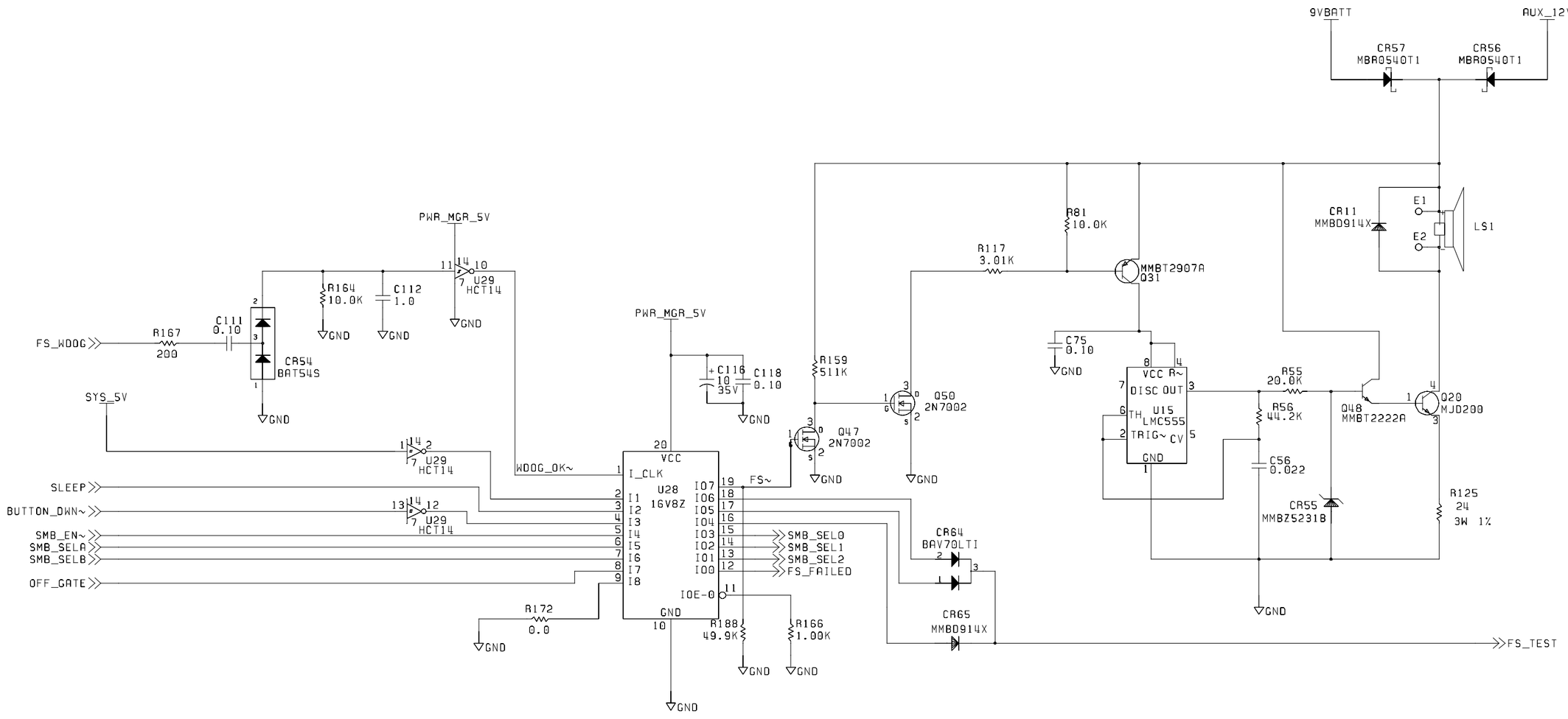
SC315-524 BA
System Support PWA Schematic (2 of 11)



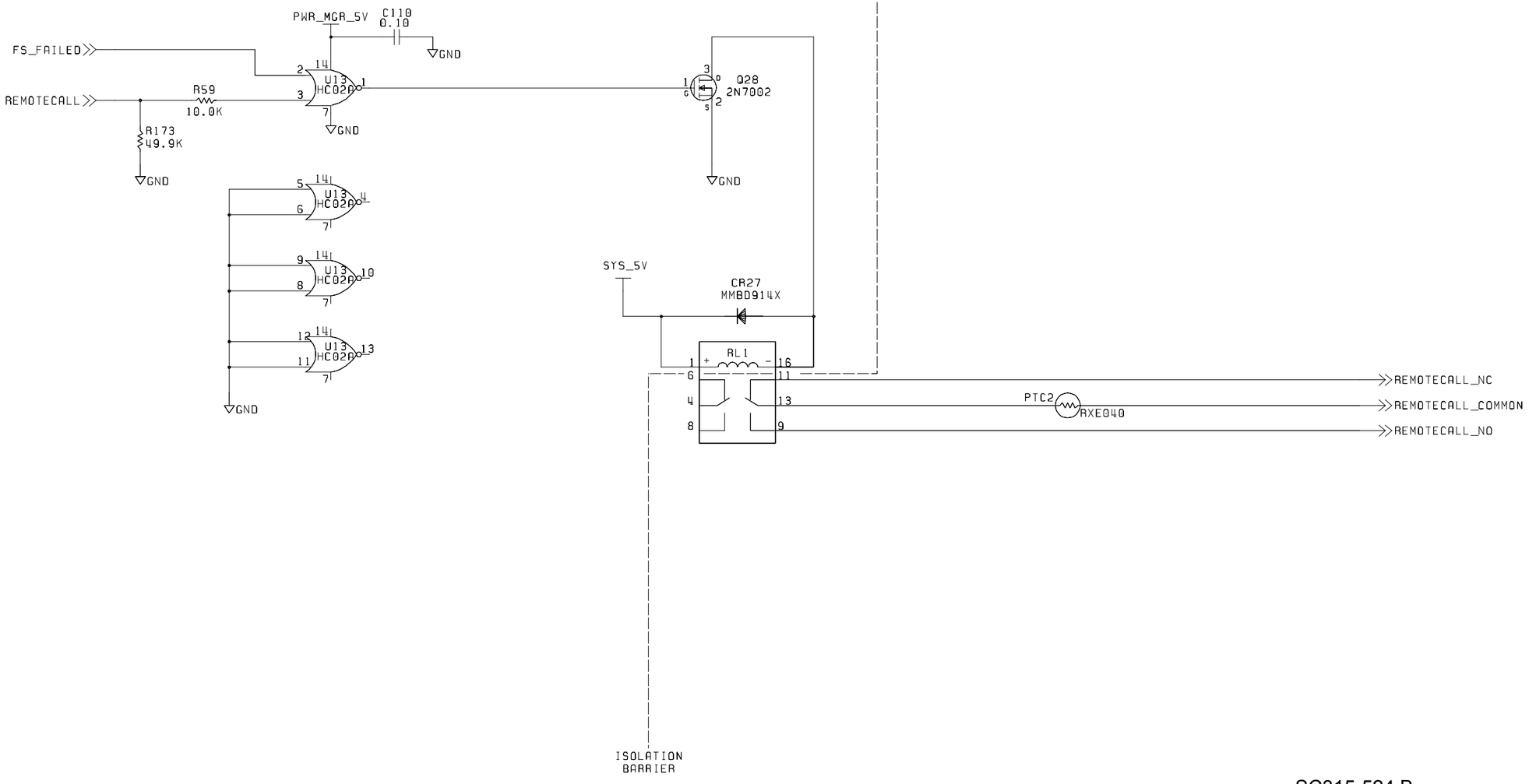
SC315-524 B
System Support PWA Schematic (3 of 11)



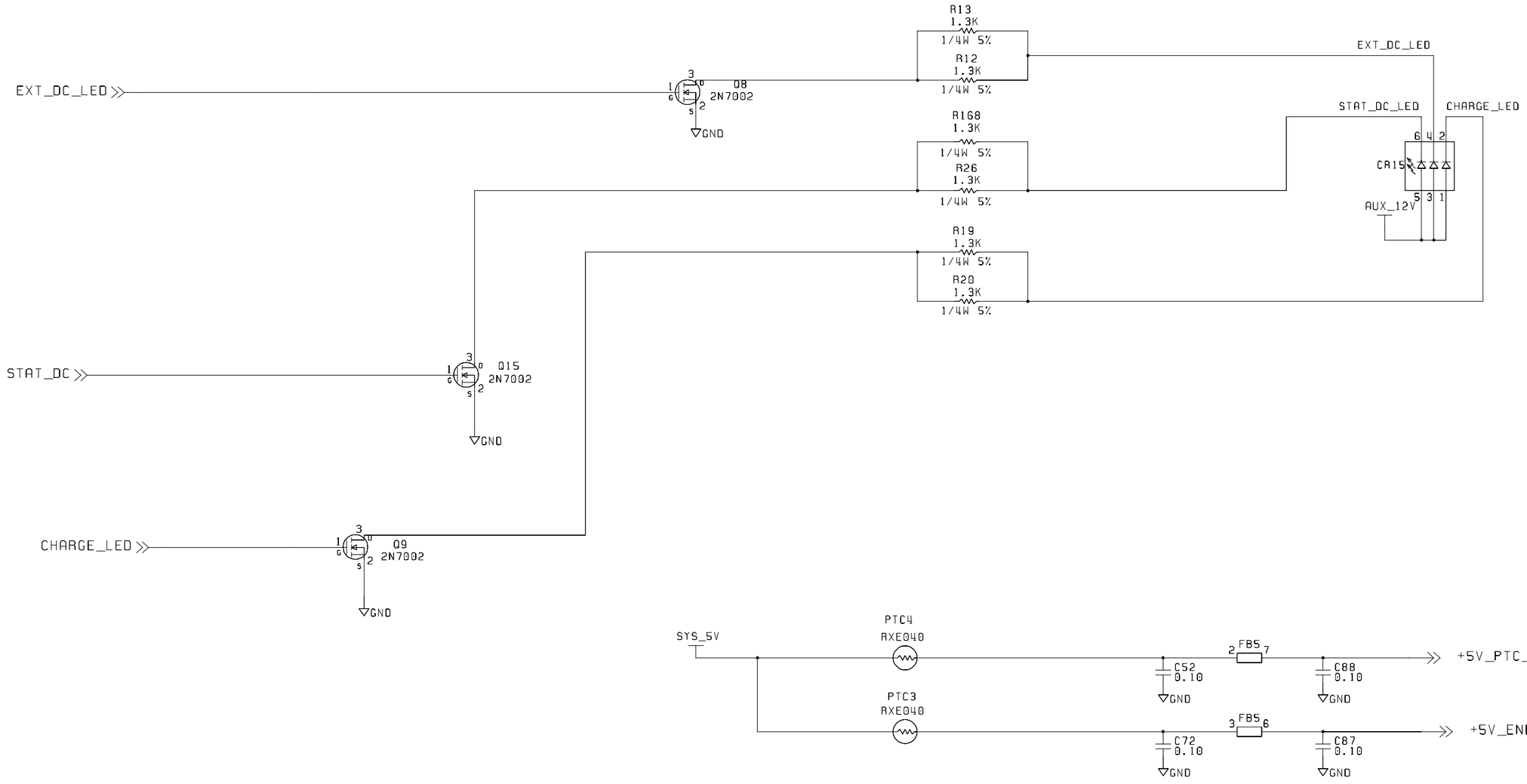
SC315-524 B
System Support PWA Schematic (4 of 11)



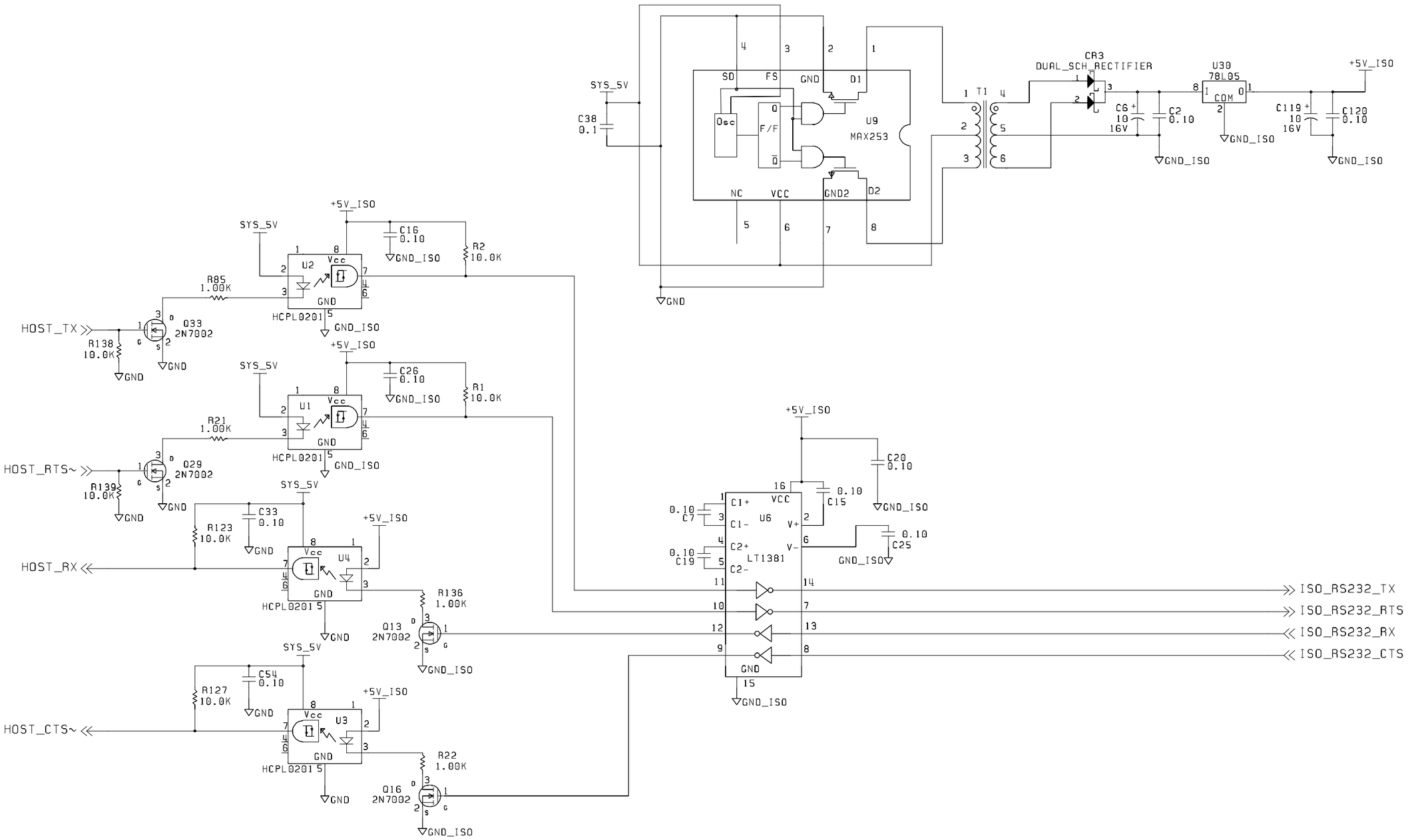
SC315-524 B
System Support PWA Schematic (5 of 11)



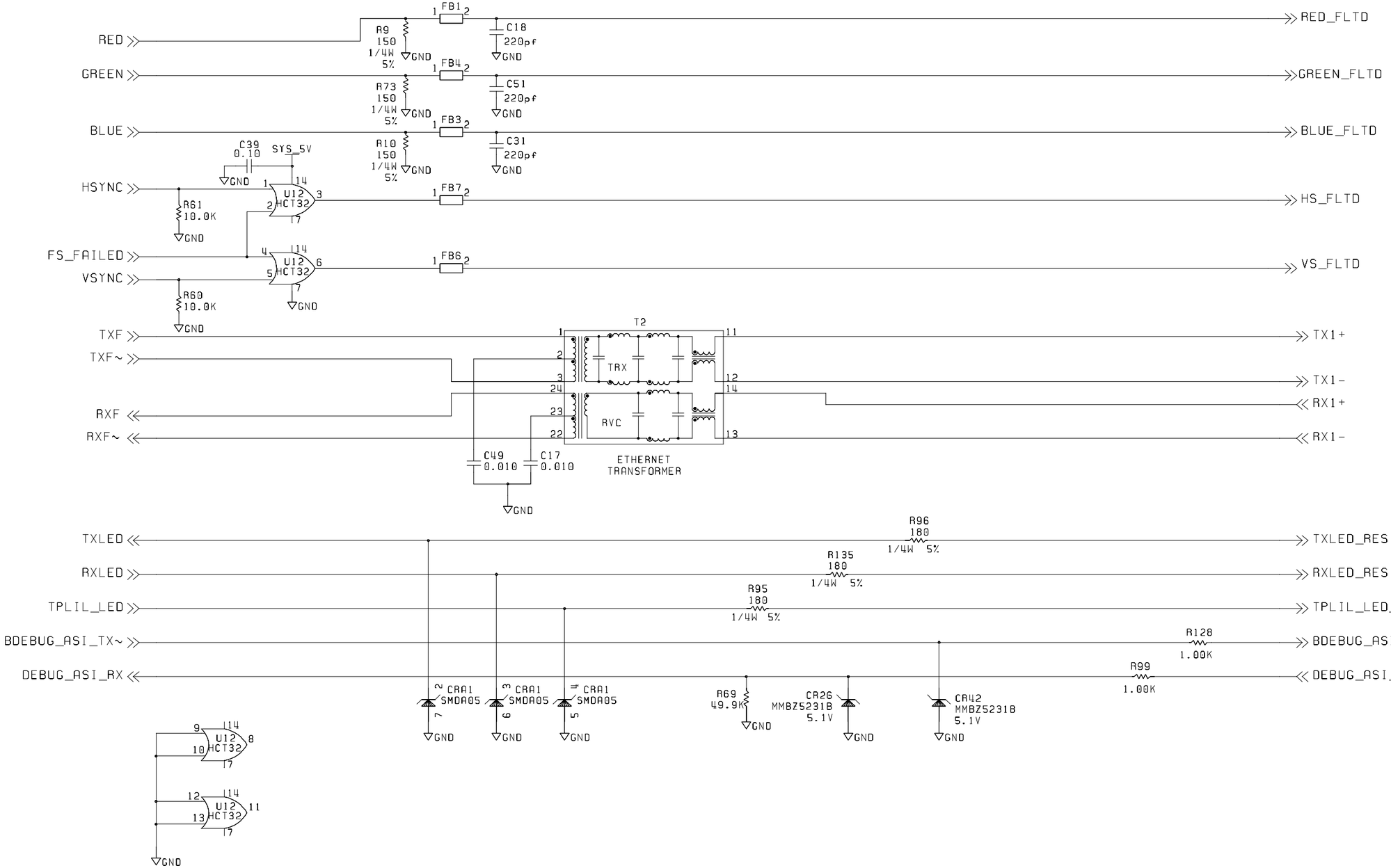
SC315-524 B
System Support PWA Schematic (6 of 11)



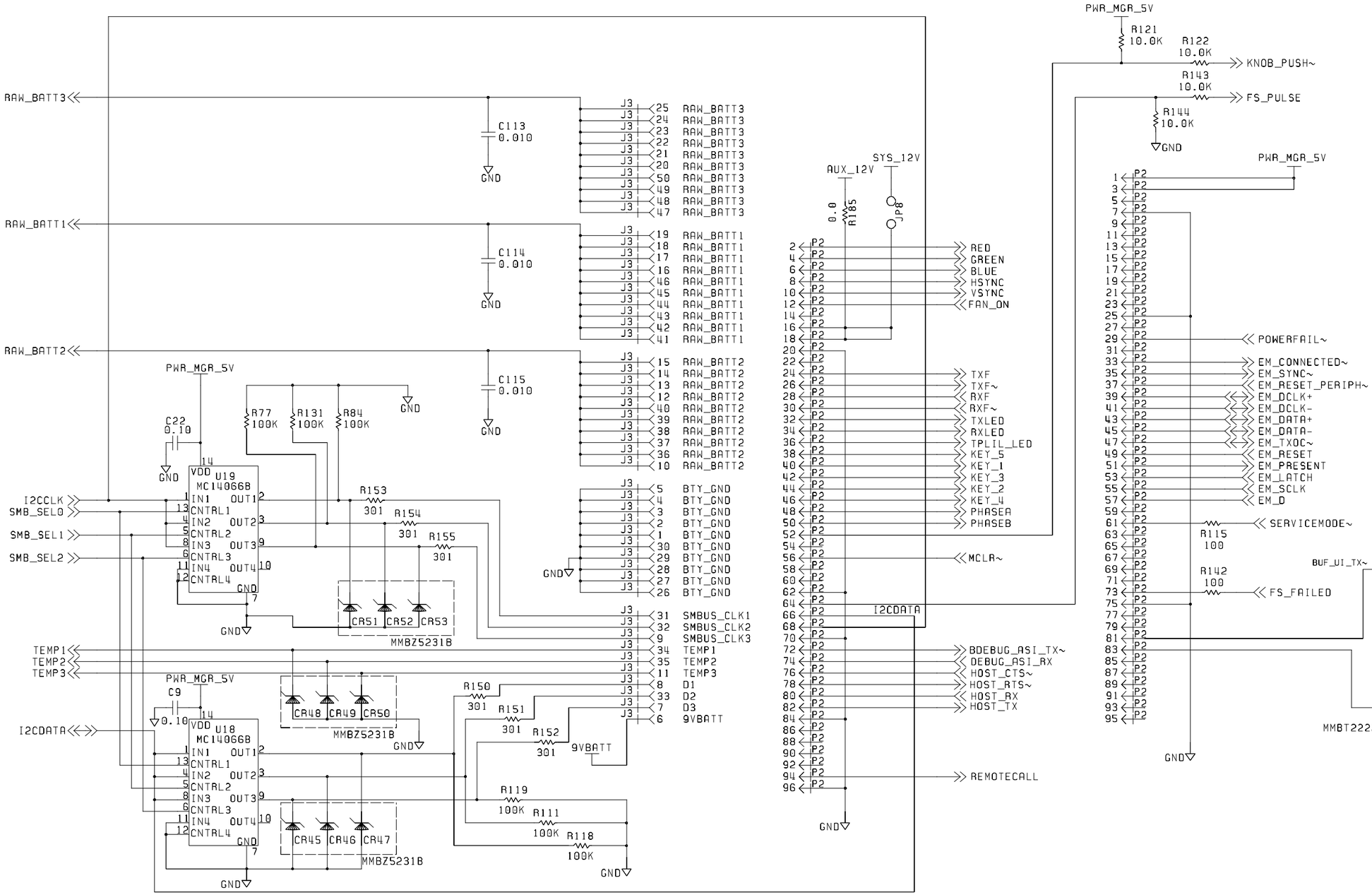
SC315-524 B
System Support PWA Schematic (7 of 11)



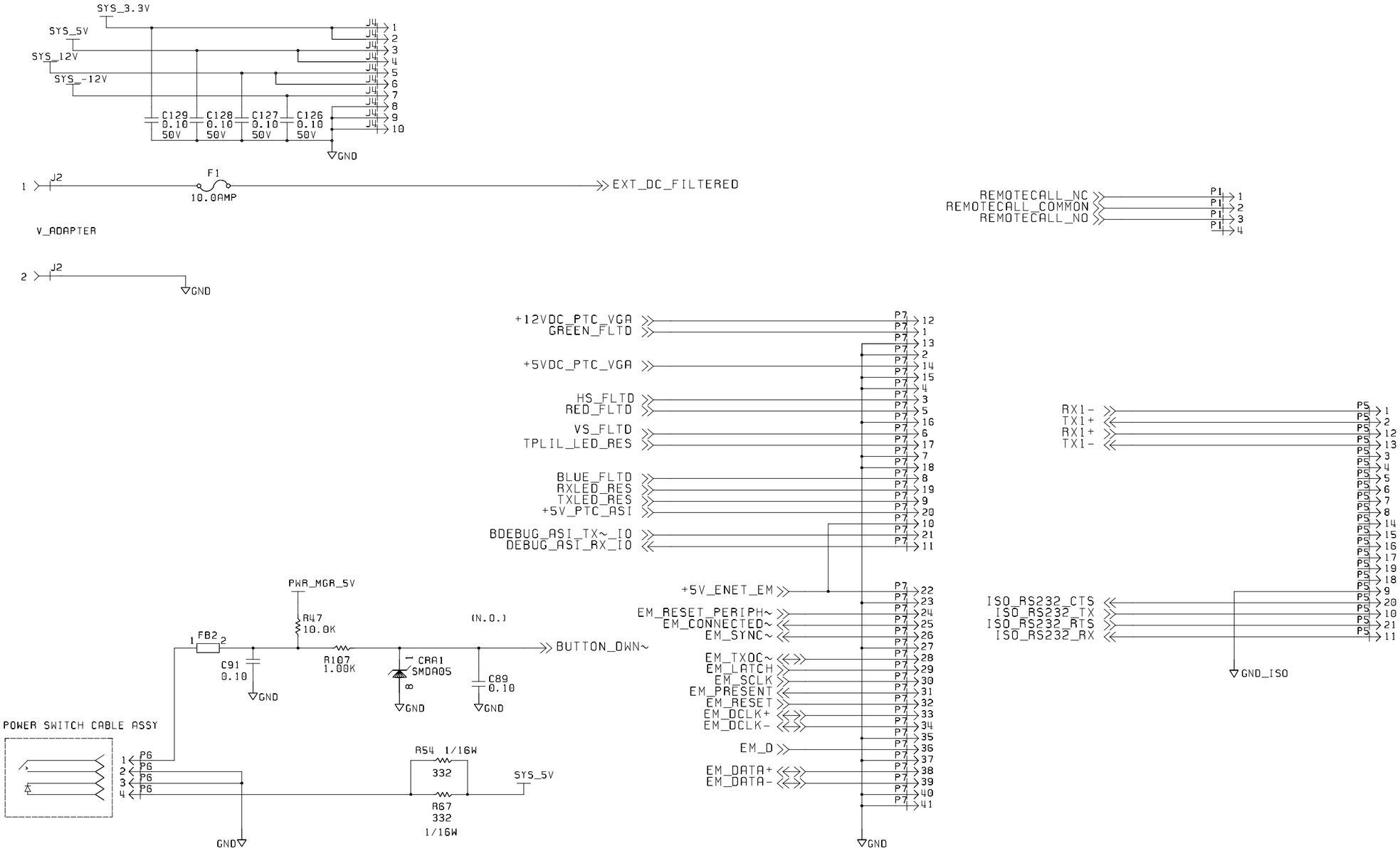
SC315-524 B
System Support PWA Schematic (8 of 11)



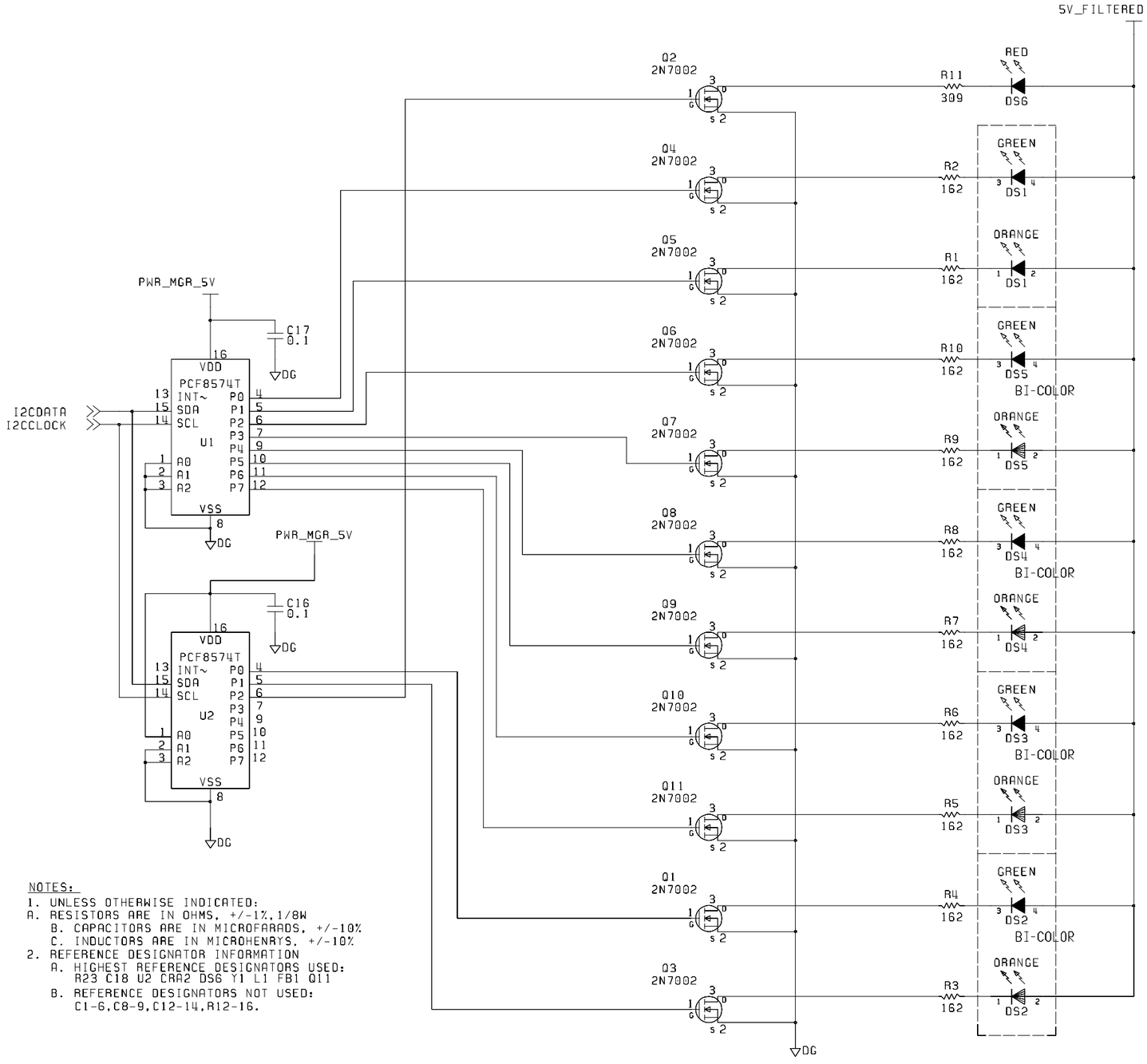
SC315-524 B
System Support PWA Schematic (9 of 11)

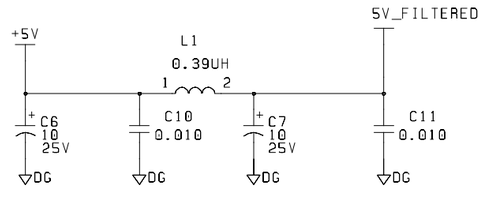


SC315-524 B
System Support PWA Schematic (10 of 11)



SC315-524 BA
System Support PWA Schematic (11 of 11)

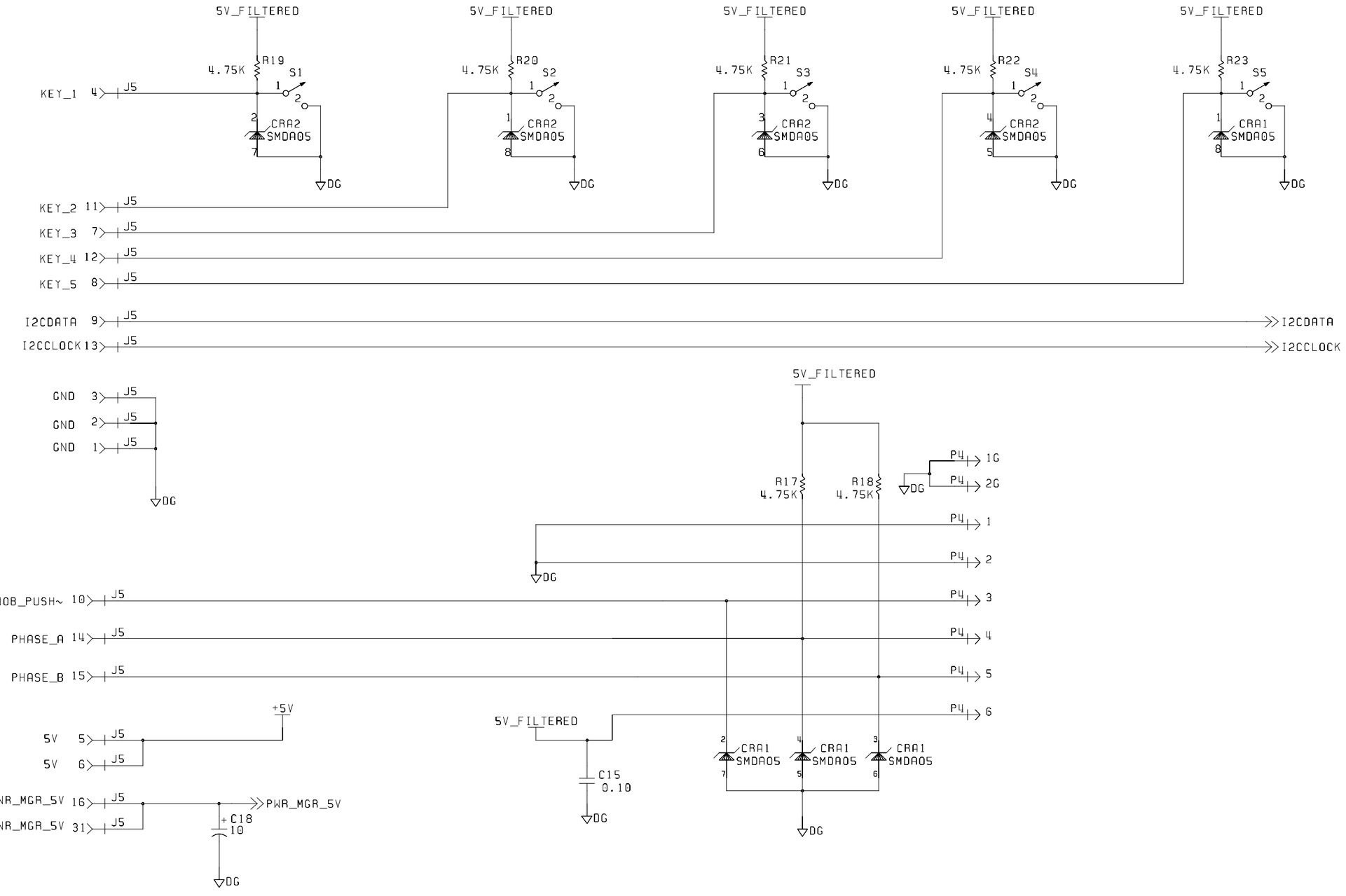




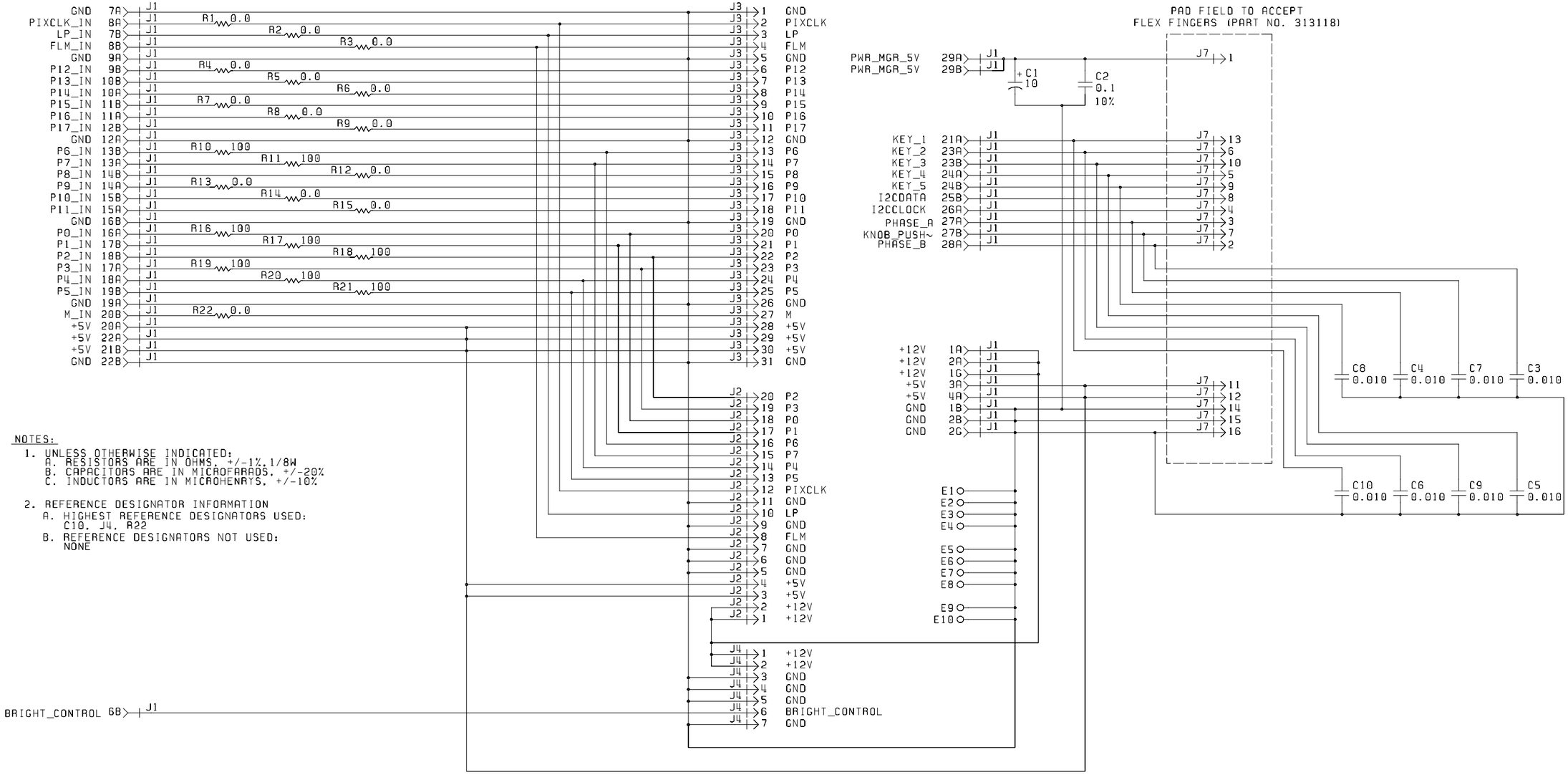
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/8W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      R23 C18 U2 CR2 DS6 Y1 L1 FB1 Q11
   B. REFERENCE DESIGNATORS NOT USED:
      C1-6,C8-9,C12-14,R12-16.

SC315-530 A
User Interface PWA Schematic (1 of 2)



SC315-530 A
User Interface PWA Schematic (2 of 2)



NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/8W
   B. CAPACITORS ARE IN MICROFARADS, +/-20%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C10, J4, R22
   B. REFERENCE DESIGNATORS NOT USED:
      NONE

SC315-542 A
Interconnect PWA Schematic