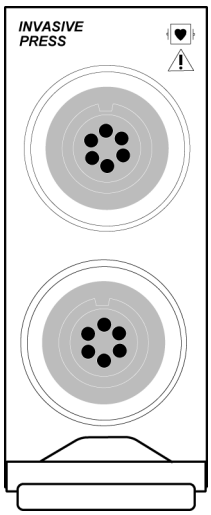
INVASIVE PRESSURE MODULE

INTRODUCTION

This area contains service information about the Model 7330 Invasive Pressure (IP) Module. The Module can monitor two channels of invasive pressure derived from resistive bridge pressure transducers. Monitored blood pressure typically includes pulmonary artery pressure or central venous pressure. Heart rate values are also determined by a weighted average formula that is applied to pulse rate data obtained from a pulsatile invasive pressure.



PHYSICAL DESCRIPTION

The IP module, shown in FO-6B, occupies a single parameter slot. The circuitry is contained on a single, 6-layer PWA. The module contains a front panel with connectors for one or two resistive bridge pressure transducers. A flex circuit PWA transfers the signals from the connectors to the rigid PWA. The two layers of the flex circuit act as a shield for the inner signal traces. Removable metal cans cover the top and bottom of the PWB isolated circuitry. The two side insulators (item 13) insulate isolated circuitry from non-isolated circuitry, and thus ensure compliance with patient safety requirements.

FUNCTIONAL PRINCIPLES OF OPERATION

A functional block diagram of the IP Module is shown in FO-6A. The diagram is divided into isolated circuitry and non-isolated circuitry. The isolated circuitry includes the EMI filters, IP front end amplifiers and filters, A/D conversion, and isolated control. The ISO interface and DC-DC converter isolate this circuitry from the non-isolated core logic.

The core logic provides communication between the system host and module through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the pressure channels.

Isolated Circuits

Isolated circuits are shown in the top half of FO-6A. Signals from pressure transducers at two patient connections are received through the module front panel connectors and are connected to the circuit board via a flex circuit. IP1 and IP2 are then filtered and applied to the IP front end.

The IP front end supplies ratiometric excitation (IPEX) to the transducers via the EMI filter and amplifies the IP1 and IP2 input from the pressure transducer bridge. Disconnect signals (DIS_CON) are used to determine when a transducer has been plugged in.

The A/D Conversion block samples analog data IP1 and IP2. A buffered version of the A/D reference is used for transducer excitation. This allows the readings to be isometric. The A/D converter is controlled by the isolated control FPGA.

The ISO control FPGA receives serial commands from the CPU and reports status and sends data back to the CPU through the ISO interface. The ISO interface provides an isolated asynchronous serial communication channel between the core logic and the isolated control FPGA.

The isolated power block consisting of +9V, +5V, -9V, and -5V power supplies provides isolated power to the patient connected circuitry.

Non-Isolated Circuits

Non-isolated circuits are shown in the bottom half of FO-6A. Functional blocks include the PNet interface, reset/failsafe, 68302 microprocessor, 8 bit memory, and logic analyzer/test interface.

Power for the core logic (+12V and +5V), is received through J1. The +12V is applied to the DC-to-DC converter which powers the isolated power block. The +5V supplies power to all non-isolated core logic. The -12V and +3.3V power supplies are not used on this Module.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a module are limited to a peak inrush current during hot-plugging. Within 2 seconds the module responds to identification and wakes up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for test and development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafe if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

IP Module PWA schematic SC315-447 and IP Flex PWA schematic SC313-104 are contained here. The first two sheets of SC315-447 show an overall block diagram of the IP PWA.

EMI Filtering

The EMI filter circuit is shown on sheet 3 of the schematic. Transducer signals are received on front end connector J100 (sheet 1) with the following pinout:

PIN	NAME	PIN	NAME
1	IPEX2-_RAW	5	IP1+_RAW
2	IP2+_RAW	6	IPEX1-_RAW
3	IP2-_RAW	7	IPEX1+_RAW
4	IPEX2+_RAW	8	IP1-_RAW

The transducer plug shield is connected to shield ground (SGRD). SGRD is terminated to ground (IG) by a 10KΩ resistor. Filtering on all transducer signals is accomplished by a ferrite core encircling the flex, providing common mode filtering. Also, 1000 pf bypass capacitors C149 through C152 and C154 through C157 decouple each signal to the internal shield. These signals are clamped at ±9V by CR13 and CR14. As shown on sheet 4, the input signals IP1+/- and IP2+/- have additional lower frequency common mode filtering through C125, C126, C130, and C131, and differential mode filtering through C122 and C147.

IP Front End

The IP front end amplifies and filters the input from the pressure transducer bridge. The IP front end is shown on sheet 4 of the schematic.

Pressure Channels

Excitation drivers U124-5,6,7 and U123-1,2,3 buffer and scale AD_REF from the A/D converter to provide a nominal transducer voltage excitation of +4.97V (IPEX1+ and IPEX2+) for both pressure transducers. This gives a nominal scale of 24.85 µV/mmHg at the input, for a transducer which has a gain of 5µV/V/mmHg. Since the excitation is derived from the A/D reference, the system is ratiometric and variations in the reference cancel. R174, C141 and R173 and C142 provide lead compensation for the excitation driver.

The bridge outputs from the transducers are received differentially through instrumentation amplifiers U100 and U101. The dynamic range of the channel is nominally an input pressure of ±500 mmHg. The instrumentation amplifiers have a gain of 100. The pressure channels (IP1 and IP2) are then passed through 4-pole, low pass, 40 Hz Butterworth anti-aliasing filter U119, with an additional gain of 1.638. The two pressure channels (IP1 and IP2) are then multiplexed and buffered where they are presented to the A/D for conversion. An IP1 or IP2 output of ≈800 mV is equivalent to 200 mmHg.

Disconnect Detection Circuitry

DIS_CON_1 and DIS_CON_2 are buffered versions of the common mode transducer bridge voltages. When an IP cable is disconnected, this voltage is pulled to the negative supply (-5V) via 10 MΩ pull-down resistors R187 and R189. Pull-down resistors are used on both the positive and negative inputs of the instrumentation amplifiers to minimize errors due to offsets currents through the transducer. When a transducer is plugged in, the common mode voltage is pulled up to half of the excitation voltage (+2.5V). Disconnect signals DIS_CON_1 and DIS_CON_2 are monitored via an A/D converter. A disconnected cable gives a full scale A/D reading of -2.048V, while a connected transducer is ≈ 2V.

Test/Calibration Interface

U112 consists of two double-pole double-throw analog switches are used in front of instrumentation amplifiers U100 and U101. These switch in calibration signals for channel gain and offset. The control for these signals is provided by the Isolated Control section. With IPTESTZERO-0 low, asserting IPTEST1-0 and/or IPTEST2-0 pulls both inputs of the instrumentation amplifiers to ground allowing the channel zero to be read. Releasing IPTESTZERO-0 turns on Q102 and Q103, and provides approximately 5 mV at the junction of voltage dividers R148-R146 and R154-R155. This voltage is applied through the analog switches to instrumentation amplifiers U100-3 and U101-3 when IPTEST is selected. This voltage is equivalent to 199.8 mmHg and used for a calibration signal. This allows the gain of the channels to be calibrated. Additionally, anti-aliasing filter U119 response may be checked by using the Service Mode facility to input a step function and monitor the transient response of the filter output.

A/D Conversion

The A/D conversion block samples the analog data under control of the isolated control block. This circuit is shown on sheet 5 of the 315-447 schematic.

Reference

The reference AD_REF at TP100 for the A/D is the 4.096V internal reference provided by the MAX191 A/D converter U111. The A/D reference, scaled and buffered at U123 and U124, provides the reference for the transducer excitation for both pressure transducers.

Multiplexer Control

The two pressure channels (IP1 and IP2) are multiplexed by U102 and buffered by U122 where they are presented to the A/D for conversion. Clamping diodes before the A/D buffer keep the input to the A/D within a diode drop of the supplies (±5V). The 8-to-1 multiplexer U102 controls channel selection of IP1, IP2, DIS_CON_1, DIS_CON_2, and resistor networks R108-R113. The resistor networks allow the A/D converter to monitor ±9 and -5V power supplies. The select signals, MUX0, MUX1, and MUX2 are controlled by the isolated control section. The isolated control section controls the switching of the select signals, and takes into account the acquisition and settling times needed between A/D conversions.

Converter Characteristics

A filtered version of digital power supply +5VD (+5VA) is used to power the A/D converter U111. The A/D is a bipolar 12-bit sampling converter with full scale ranging from ±2.048V. This yields approximately 4 LSBs/mmHg for the pressure channels. Digital data is output (DOUT) serially and formatted in 2's complement. The conversion rate is determined by the AD_CLK (SCLK) frequency, normally 410 kHz.

Conversion Control

Conversion is initiated by the assertion of AD_CS and the next falling edge of the clock (AD_CLK). These control signals are derived from the isolated control section. Data (AD_DATA) is valid on the AD_CLK rising edge.

Isolated Power and Interface

The isolated power block is shown on sheet 6 of the schematic. It provides power to the patient connected circuitry which is isolated from earth ground for patient safety. The isolated communication interface is shown on sheet 7 of the schematic. It provides an isolated asynchronous serial communication channel between the core logic and the isolated circuitry.

Isolated Power

The isolated power section provides patient isolation from earth ground (compliant with UL 2601 and IEC 601) by isolating the power for the patient connected circuitry.

DC-to-DC converter PM100 provides isolated, unregulated power outputs of ±12VDC (+VS and -VS) derived from the system non-isolated +12VDC supply. L1 provides common mode filtering to reduce noise generated by the DC-to-DC converter. Voltage regulators driven from the isolated supply provide regulated +5VDC, +9VDC, -5VDC, and -9VDC supplies for the isolated circuitry.

The positive regulated supplies provide open collector PWR_OK signals which are ORd together. A logic low signal indicates that one of the regulator outputs has dropped by more than 5%.

The +9VDC, -9VDC and the -5VDC supplies are scaled and monitored through the A/D converter (R108-R111 on sheet 5).

The isolated power supply is turned on when Port A bit 6 from the CPU (ISO_POWER_ON-0) is enabled (active low).

Isolated Interface

Opto-couplers U105 and U106 provide a full duplex, isolated serial channel between the non-isolated core logic and the isolated circuitry. The isolated control block receives data through opto-coupler U105 and transmits on U106. Opto-coupler U107 transmits the baud clock (16x baud rate) which provides the clock (ISO_CLK, normally 830 kHz) to the Isolated Control. Q100, Q101, and Q105 buffer the signals to the opto-couplers.

Isolated Control

The isolated control block is shown on sheet 8 of the schematic. The isolated control block accepts commands from the core logic, provides the control for the isolated circuitry, reads input data, outputs data, and commands a/d conversion. Sampled data is passed back to the core logic through this interface.

The isolated control is implemented with a field-programmable gate array (FPGA) U104. EPROM U103 stores the configuration data for FPGA U104. This data is downloaded to U104 on power up. The function of the isolated control block is to accept serial commands from microprocessor U10 via the ISO Interface and output the appropriate control signals, AD_CS, AD_CLK, and MUX 0-3 to the analog circuitry and to transmit sample data (AD_DATA) and status back to the microprocessor. This controls the MUX channel selection, the operation of the A/D converter, and the IPTEST signals.

Core Logic

The core logic is shown on sheets 9 through 13 of the schematic. The core logic provides communication between the system host and module through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the pressure channels. The module is an 8-bit version of the core logic with one 128Kx8 RAM and 128Kx8 ROM device. The microprocessor runs at 9.966 MHz.

PNet Interface

The PNet interface, shown on sheet 10 of the schematic, provides the following functions:

- RS485 drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module reset (U6 and U9), and
- Module synchronization.

Core signals are received on PNet connector J1 (sheet 2) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The IP module is designed to be hot-plugged, or inserted and removed from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect circuitry. Protective impedance located on the system backplane, in series with the modules +5V and +12V power, limits inrush current on hot-plugging or live insertion. Series impedance on PNet control lines also limits inrush and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. The device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the module is disabled unless the module has been commanded to transmit per the PNet protocol. The module transmitter is immediately disabled after the last character of a transmission has been sent.

The module select input (M_SELECT, hi true) instructs the module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, a module performs a hardware reset.

The module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the module is plugged into an instrument. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

A low true open collector signal TXOC-0 from Q1 signifies the module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

M_SYNC is a signal used for timing purposes that require shorter latency time than supported by the serial data protocols. M_SYNC is not asserted by a Module unless enabled to do so by the host. At the time of publication, the IP Module does not drive M_SYNC.

Reset Logic

The reset logic is shown on sheet 11 of the schematic. Power on reset is generated by U9 when the unit is powered up. Processor reset (RESET-0) and halt (HALT-0) are generated by the system. RESET-0 AND HALT-0 signals remain low for minimum of 130 msec after all logic rail is in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset asserted. Power monitoring, processor reset, and halt signals low when logic rail drops below specification. they remain low for minimum of 130 msec after logic rail returns to specified range.

The reset circuit (U6-4,5,6; U6-11,12,13) provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-Safe Logic

Fail-safe latch (U6-1,2,3; U6-8,9,10 on sheet 11) ensures that the module enters a safe state should the processor fail to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled and module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor

The core logic design is based around the 68302 microprocessor (U10) shown on sheet 12 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address and data lines and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory

Program memory consists of 8-bit flash ROM U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx8 (1024k bit). The ROM is not socketed and can not be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory

Data is stored in 128Kx8 static RAM U3. This RAM is cleared when power is removed.

Non-Volatile Memory

Serial EEPROM U1 is a 128-byte PROM that provides non-volatile storage for model and serial number information and parameter user interface data which must travel with the module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface

The logic analyzer/test interface is shown on sheet 9 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the FLASH devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector. The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45,46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove two 4-40 x 5-1/4" screws from rear of the Module. Remove rear cover.
2. Slide enclosure toward rear of Module, and remove enclosure.
3. Unsnap two tabs at top and two tabs at bottom of assembly, and remove insulators and card guides.
4. Remove the 4-40 x 1/4 screw (19, FO-6B) that fastens flex cable to the shield can.
5. Lift the connector lock on J100, and pull upward on flex cable.
6. Separate front cover from PWA.
7. Using FO-6B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. Slide IP PWA into the left slot (viewed from front) of front panel.

2. Carefully insert front flex assembly into connector J100 on PWA. While holding flex circuit cable inside connector, push down on top of connector to lock flex cable in place.

3. Using 4-40 x 1/4 screw (19, FO-6B) and washer (18), secure flex terminal to ground shield on PWA. Tighten the screw to 4-in/lb.

4. Push upper and lower card guides onto slots of assembly.

5. Install insulators (13) so large notch end is toward rear of Module, to ensure integrity of patient safety isolation.

6. With enclosure oriented so large groove is at bottom and label is at right (viewed from front of Module), slide enclosure over front cover and assembly.

7. Install rear cover on the Module enclosure, making sure the ground spring makes contact to the PWA ground pad.

8. Fasten the front and rear covers to the enclosure by inserting two 4-40 x 5-1/4" screws from the rear through the enclosure to the front cover as shown in FO-6B. Tighten the two screws to 4-in/lb.

PARTS LISTS

Top Assembly 7330 parts are listed in Table 6-1 and shown in FO-6B. Invasive Pressure PWA 315-447 parts are listed in Table 6-2 and shown in FO-6C. IP Flex PWA 313-104 parts are listed in Table 6-3 and shown in FO-6D.

Table 6-1. Top Assembly 7330 Parts List

Item	Description	Part No.
1	COVER, PARAMETER REAR	703-188
4	EMI SHIELD, INTERNAL, PWA, IP	737-178
5	PWA, FLEX, INVASIVE PRESSURE	313-104
6	EMI SHIELD, EXTERNAL, PWA	737-179
7	PWA, INVASIVE PRESSURE	315-447
8	EMI GASKET, SHIELD, PWA	737-180
9	PANEL, FRONT, INVASIVE PRESSURE	701-428
10	SCREW, RDH PHH, 4-40X51/8, CUSTOM	722-201
11	INSULATION, GUIDE, MODULE	750-182
12	SUB-ASSY, ENCLOSURE, EXTRUDED SW	320-676
13	INSULATOR, DIGITAL	750-189
15	GASKET, CONNECTOR, FRONT PANEL	752-262
16	BUTTON, LATCH, SW	732-166
17	SPRING, CONTACT, GROUND	736-204
18	WASHER,FLAT #4 SST	723-403
19	SCREW, 4-40X1/4 PNH PHH SST	719-102
20	SCREW, 2-56X3/16 PNH PHH SST	719-237

Table 6-2. Invasive Pressure PWA 315-447 Parts List

Item	Description	Part No.
C1,169,172, 173,176,178	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C2,3,190,191	CAP,CER,SMD,0603,NPO,10%,50V,27 PF	605-718
C4-14, 16, 101-108, 111, 113, 115-121, 123-126, 130-134, 136-138,140, 145,146,148, 187,188,192	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C109,112,128 ,129	CAP, POLYCARBONATE, .047UF, 100V, 5MM	603-211
C110, 139, 143, 144	CAP, POLYCARBONATE, .015UF, 100V, 5MM	603-212
C114	CAP,CER,SMD,0603,X7R,10%,50V,0.010 UF	605-821
C122,127	CAP,CER,SMD,0805,X7R,10%,50V,0.047 UF	605-529
C136-138,140, 145,146,148, 187,188,192	CAP,CER,SMD,0805,X7R,10%,50V,0.010 UF	605-533
C141,142	CAP,CER,SMD,0603,NPO,10%,50V,10 PF	605-713
C160	CAP,2312/C,TANT,16V20%4.7UF	606-106
C161,162,170 ,171	CAP,2312/C,TANT,16V,20%,10 UF	606-108
C163-166	CAP,1206/A,TANT,20V,20%,1.0UF	606-128
C179-186	CAP,CER,SMD,0805,X7R,10%,50V,0.010 UF	605-521
C189	CAP,CER,SMD,0603,NPO,10%,50V,100 PF	605-725
CR1,13,109, 110,112, 115,120	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7,10,11, 113,114	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
CR108,111	DIODE, RECT-SCHOTTKY, 1A, 40V, SMT	611-142
CR116-119	DIODE, LOW LKG, DUAL SMT MMBD1503A	610-140
FB1-8	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J1	CONN, 20 PIN PLUG RT ANGLE PC MOUNT	607-795
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
J100	CONN, 8 POSN, 1MM, ZIF, SMT	607-902
L100	FILTER, DATA LINE (3-LINES)	668-162
PM100	PWR SUPPLY, DC TO DC 1.5W PC MT	633-147

Table 6-2. Invasive Pressure PWA 315-447 Parts List (Continued)

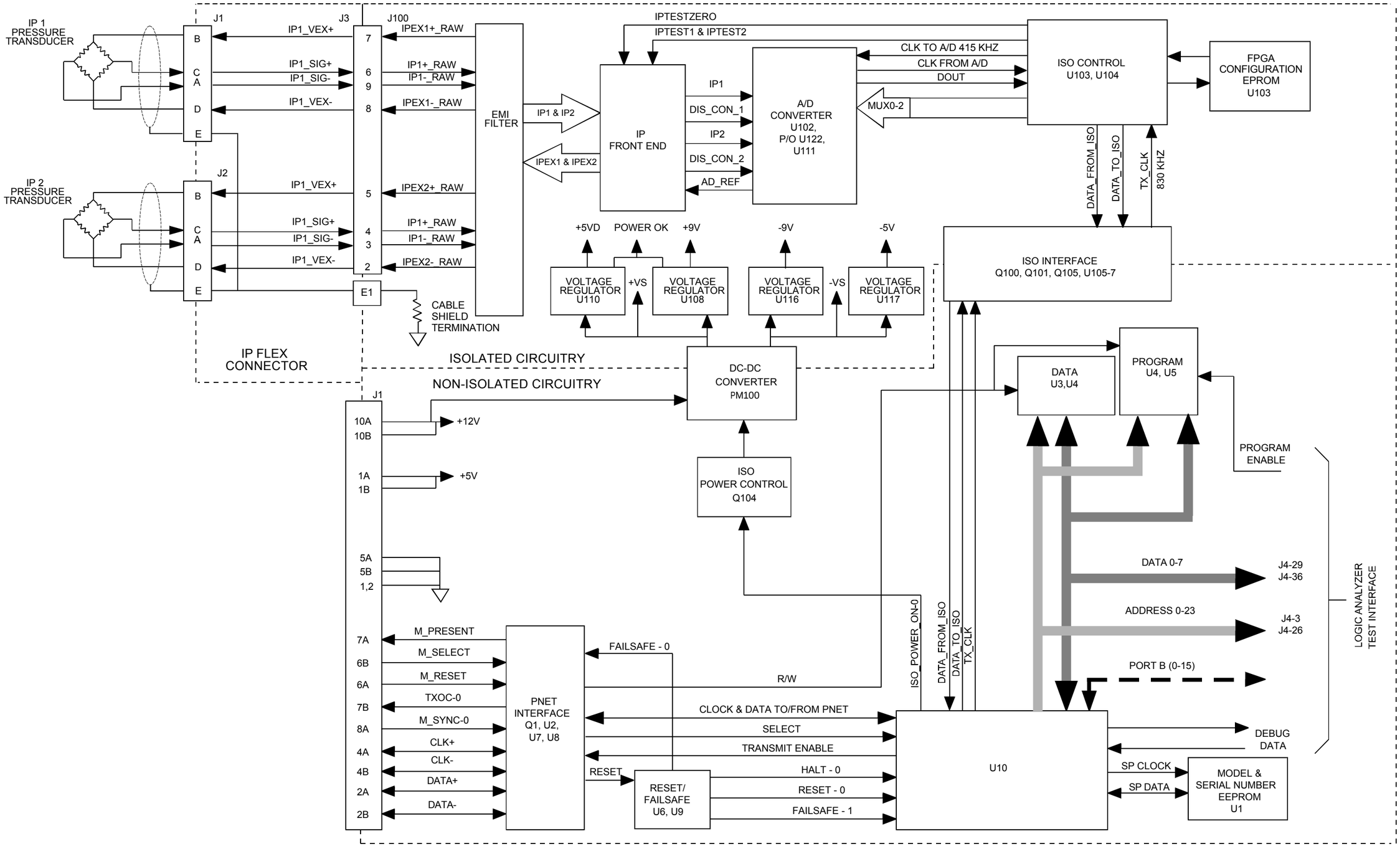
Item	Description	Part No.
Q1	XST NPN 2222A SMT	674-127
Q100-105	XSTR, N-CHAN MOS SOT-23	676-130
R1,40,41,44, 50,119,120, 142,145, 164,195	RES,SMD,1/10W,1%,1.00K OHM	685-293
R2	RES,0603,1/16W,1%,4.99K OHM	686-360
R3,4,7-33,35 42,43,46-48, 100-102,110, 112,121, 129-136,143, 144,163, 191-194	RES,0603,1/16W,1%,10.0K OHM	686-389
R5,6	RES,0603,1/16W,1%,2.21K OHM	686-326
R34	RES,0603,1/16W,1%,698K OHM	686-566
R45	RES,SMD,1/10W,1%,100 OHM	685-197
R105,183	RES,0603,1/16W,1%,4.02K OHM	686-351
R108,111,113 ,123,167, 171,172	RES,0603,1/16W,1%,73.2K OHM	686-472
R109,166,181	RES,0603,1/16W,1%,30.1K OHM	686-435
R118,178	RES,0603,1/16W,1%,118K OHM	686-492
R122,168, 176,177	RES,0603,1/16W,1%,20.5K OHM	686-419
R124,170	RES,0603,1/16W,1%,46.4K OHM	686-453
R125,180	RES,0603,1/16W,1%,487K OHM	686-551
R126,200-203	RES,0603,1/16W,1%,110K OHM	686-489
R127,156, 173,174	RES,0603,1/16W,1%,24.9 OHM	686-139
R128	RES,0603,1/16W,1%,649K OHM	686-563
R140,141,162	RES,SMD,1/10W,1%,475 OHM	685-262
R146,155	RES, SMT, 100 OHM, .25%, 50 PPM/C	687-102
R147,151	RES,0603,1/16W,JUMPER 0.0 OHM	686-606
R148,154	RES, SMT, 100 KOHM, .25%, 50 PPM/C	687-103
R149,187-189	RES,SMD,1/10W,5%,10M OHM	685-605
R157,158	RES,0603,1/16W,1%,49.9K OHM	686-456
R159	RES,0603,1/16W,1%,316K OHM	686-533
R163,191-194	RES,0603,1/16W,1%,10.0K OHM	686-389
R169,179	RES,0603,1/16W,1%,187K OHM	686-511
R175,182	RES,0603,1/16W,1%,140K OHM	686-499

Table 6-2. Invasive Pressure PWA 315-447 Parts List (Continued)

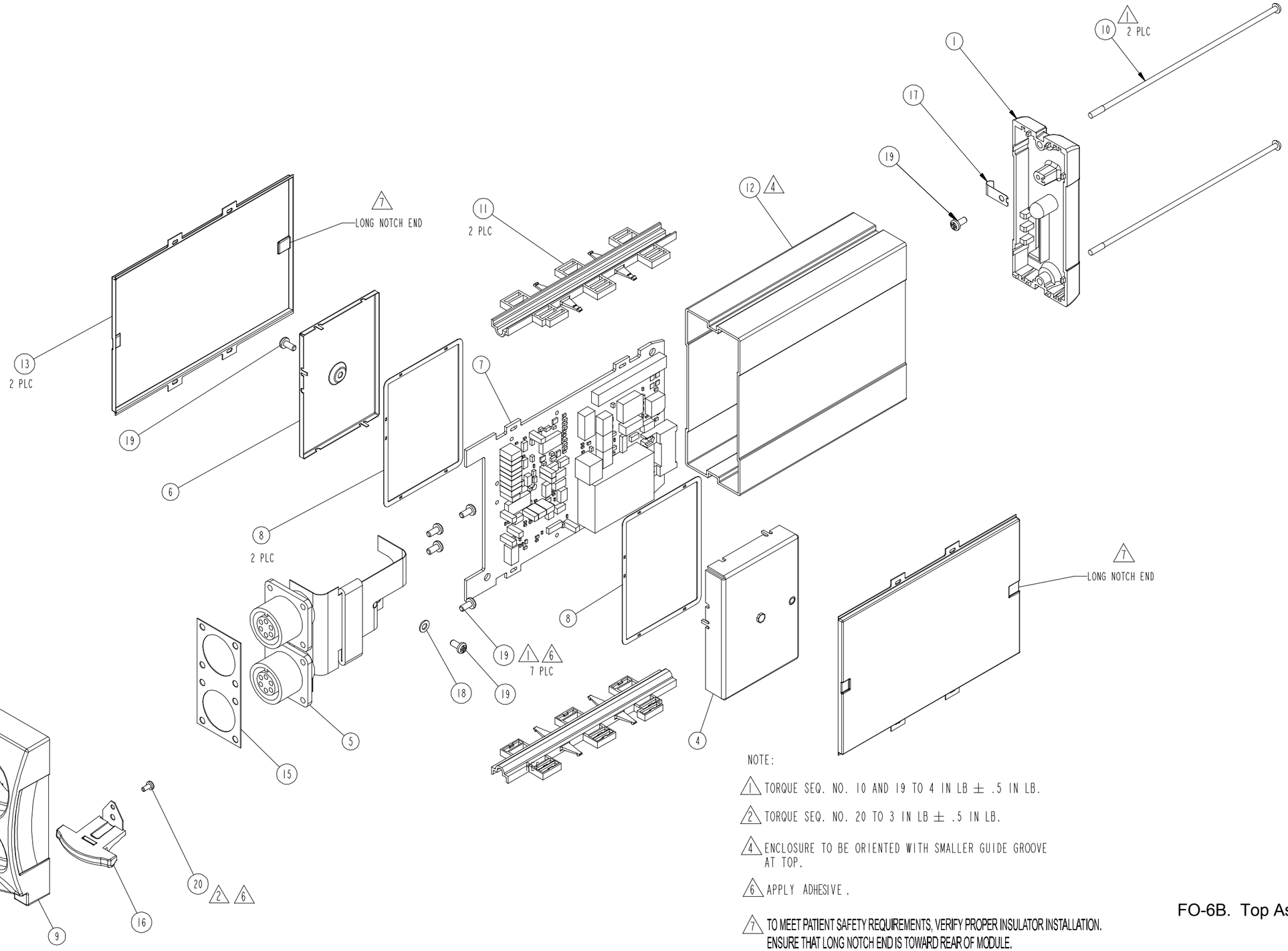
Item	Description	Part No.
R190	RES,0603,1/16W,1%,10.0 OHM	686-101
R197-199	RES,0603,1/16W,1%,100 OHM	686-197
TP100,109	CONN, 2 POSN HEADER, .025 SQ	608-287
TP102	CONN, 5 POSN HEADER, 0.025 SQ	608-303
TP105,111, 112,114,117	CONN, 1 POSN HEADER, .025 SQ	608-288
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U3	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U4	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141
U5	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7,8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 INTEGRATED PROCESSOR 144 SMT	694-130
U100,101	IC, INSTR AMP, 50-8	691-122
U102	IC, ANALOG MUX, CMOS SO-16	693-126 or 692-239
U103	IC, EPC1064 SERIAL EPROM 65K BIT	619-264
U105-107	IC, HCPL-2611, OPTOCOUPLERS, SMT	695-101
U108,110	IC, ADJ VOLTAGE REGULATOR SMT	693-119
U111	IC, MAX191 12 BIT ADC, CMOS SMT	692-199
U112	IC, MAX333A QUAD SPDT CMOS ANA SW SMT	692-201
U116,117	IC, 664 VOLTAGE REGULATOR SUR. MT.	693-104
U119	IC, QUAD OP AMP SUR. MT.	691-119
U122	IC, HS, LP, OP AMP, SOIC	691-115
U123,124	IC, DUAL JFET OP AMP, S0-8	691-116
U134	IC, CMOS PROGRAMMABLE LOGIC DEVICE SMT	692-236
U135	IC, HEX SCHMITT-TRIGGER INVERTER, SMT	692-237
Y1	CRYSTAL, 9.966MHZ, 0.005% HC-49UP	609-128
#77	SOCKET,DIP LO-PROFILE 8 PIN	607-165
#84	FPGA, INVASIVE PRESSURE/ECG	637-116
#85	PAL_U2A, CORE LOGIC	637-101

Table 6-3. IP Flex PWA 313-104 Parts List

Item	Description	Part No.
C1-8	CAP,CER,SMD,0805,X7R,10%,50V,0.010 UF	605-521
J1,J2	CONNECTOR SHELL, FLANGED RED, 6-PIN	607-823
#2	CONTACT, SOCKET, POSTED FOR .025 SQ	608-266
#3	FERRITE CORE, FPC EMI SUPPRESSION	669-203
		or 669-204
#4	PWB, FLEX, INVASIVE PRESSURE	641-104



FO-6A. Invasive Pressure Module Block Diagram



NOTE:

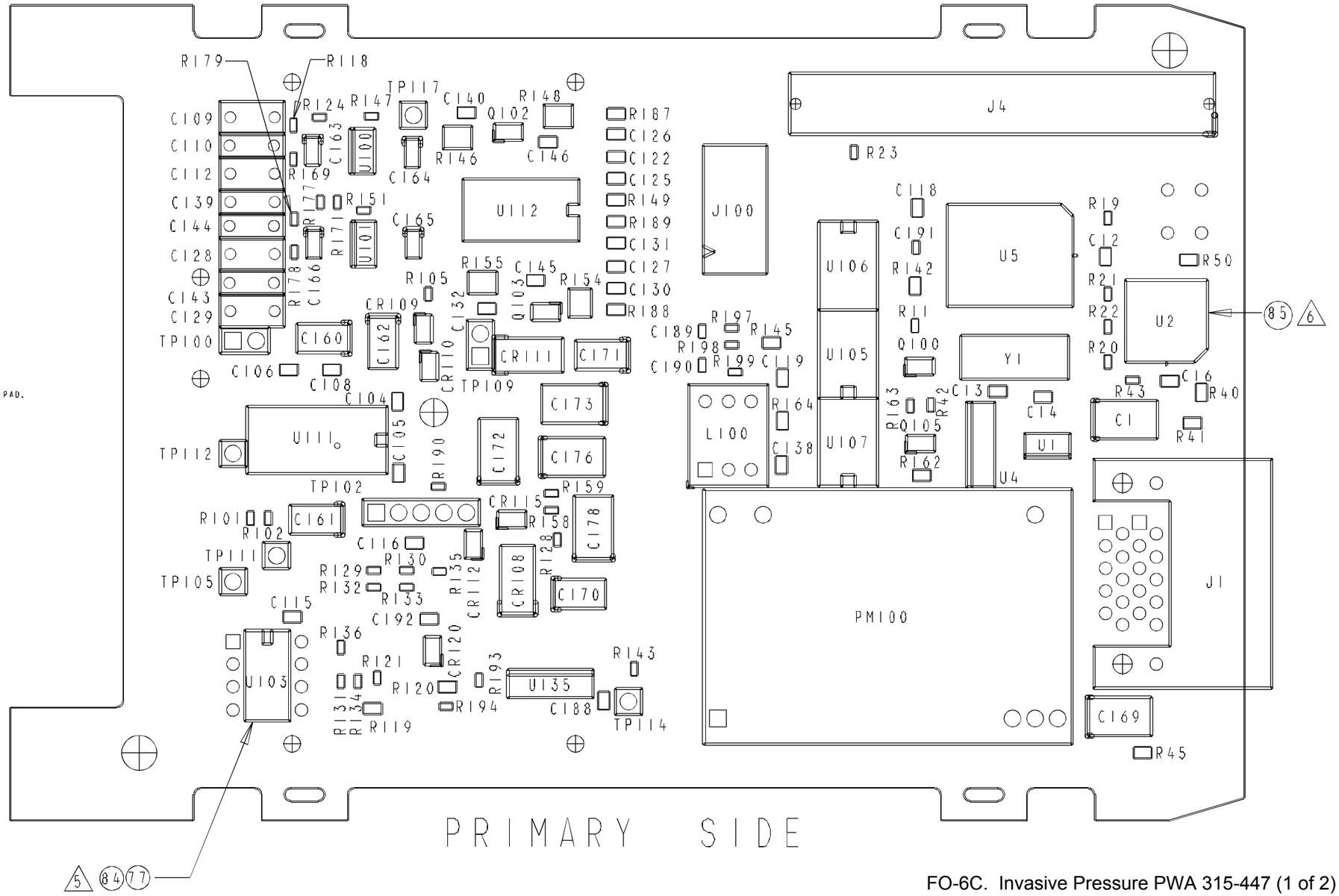
1. TORQUE SEQ. NO. 10 AND 19 TO 4 IN LB ± .5 IN LB.
2. TORQUE SEQ. NO. 20 TO 3 IN LB ± .5 IN LB.
4. ENCLOSURE TO BE ORIENTED WITH SMALLER GUIDE GROOVE AT TOP.
6. APPLY ADHESIVE .
7. TO MEET PATIENT SAFETY REQUIREMENTS, VERIFY PROPER INSULATOR INSTALLATION. ENSURE THAT LONG NOTCH END IS TOWARD REAR OF MODULE.

FO-6B. Top Assembly 7330

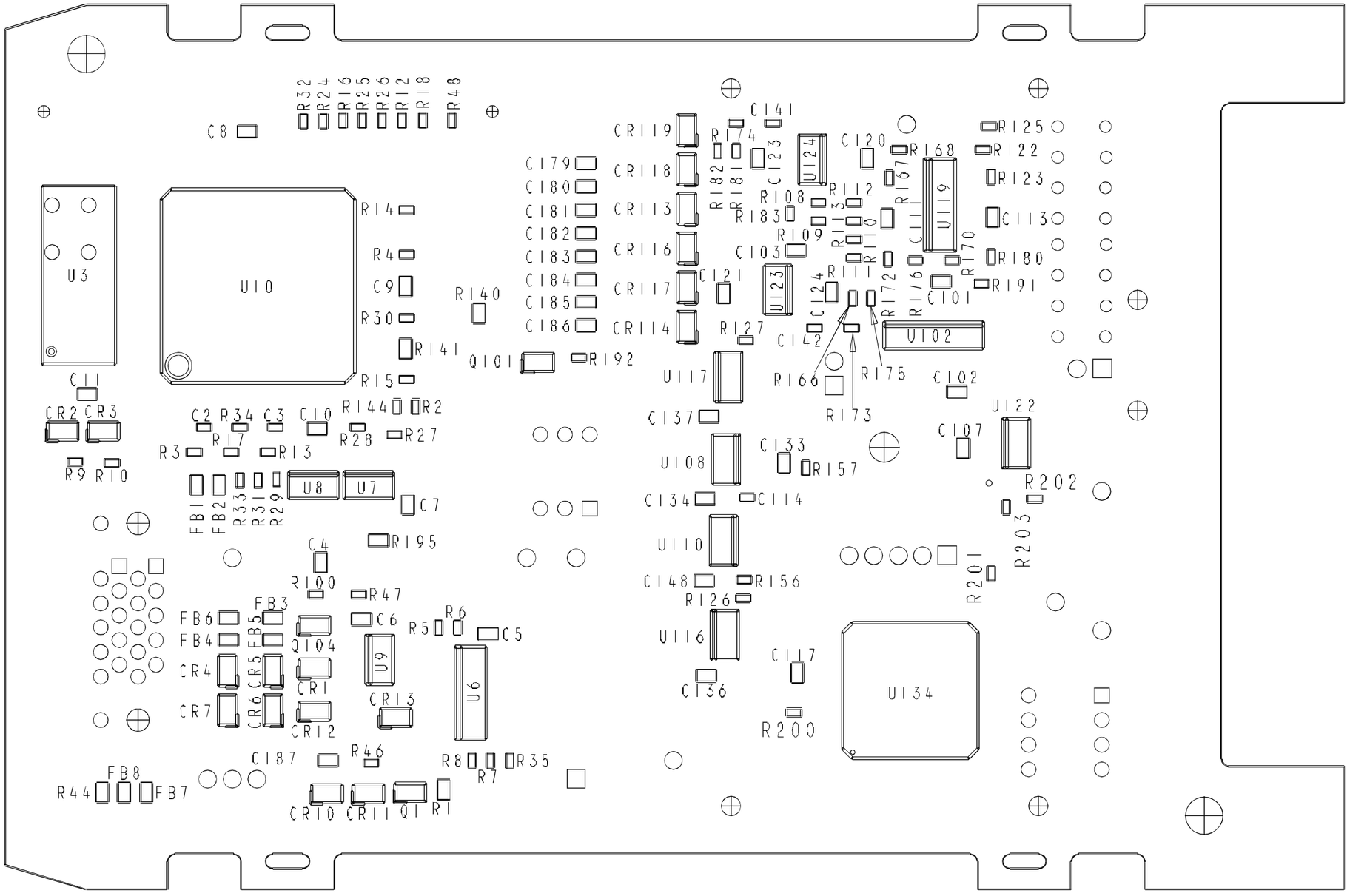
NOTES:

3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

5. 6. PROGRAM DEVICE BEFORE INSTALLATION

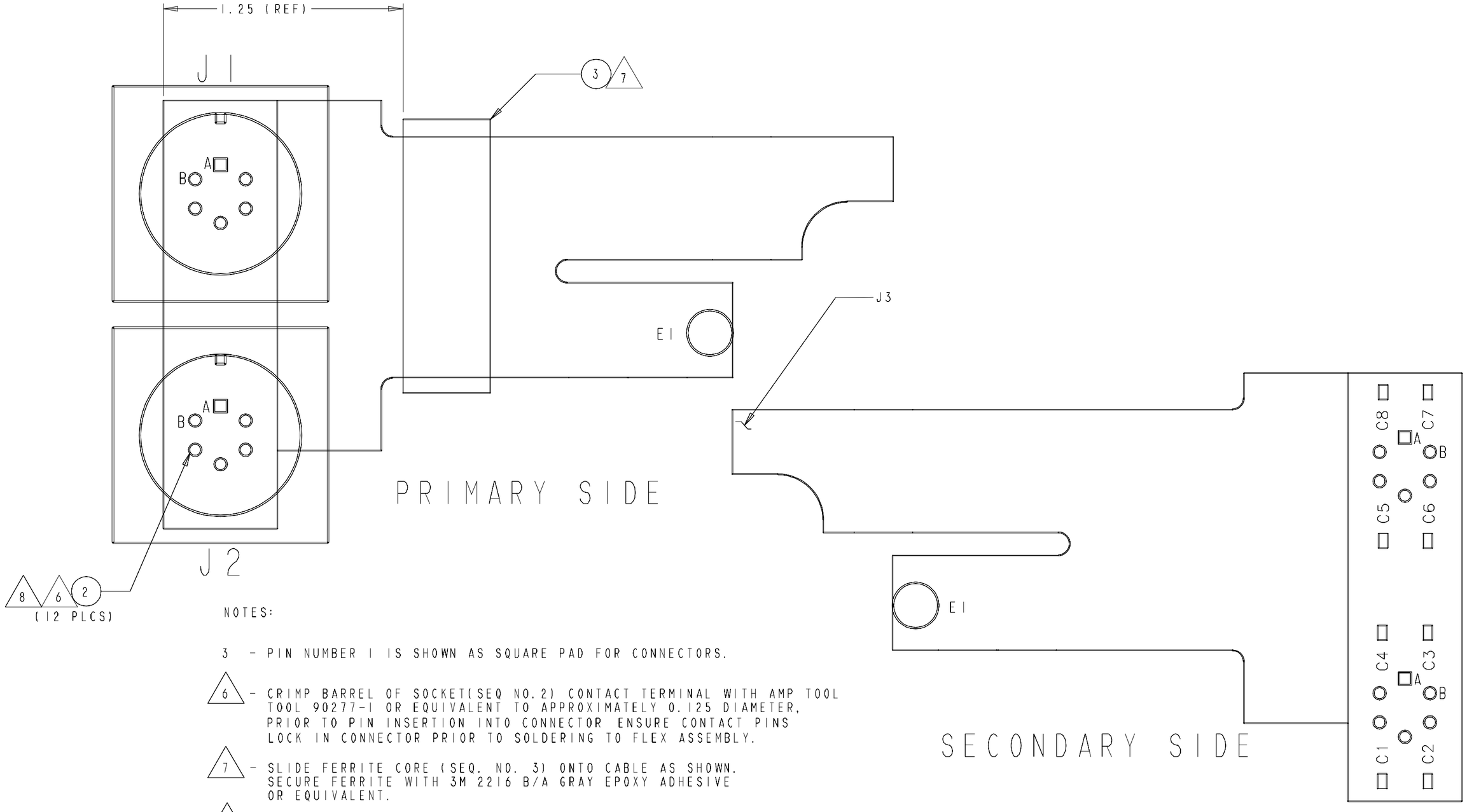


FO-6C. Invasive Pressure PWA 315-447 (1 of 2)



SECONDARY SIDE

FO-6C. Invasive Pressure PWA 315-447 (2 of 2)



NOTES:

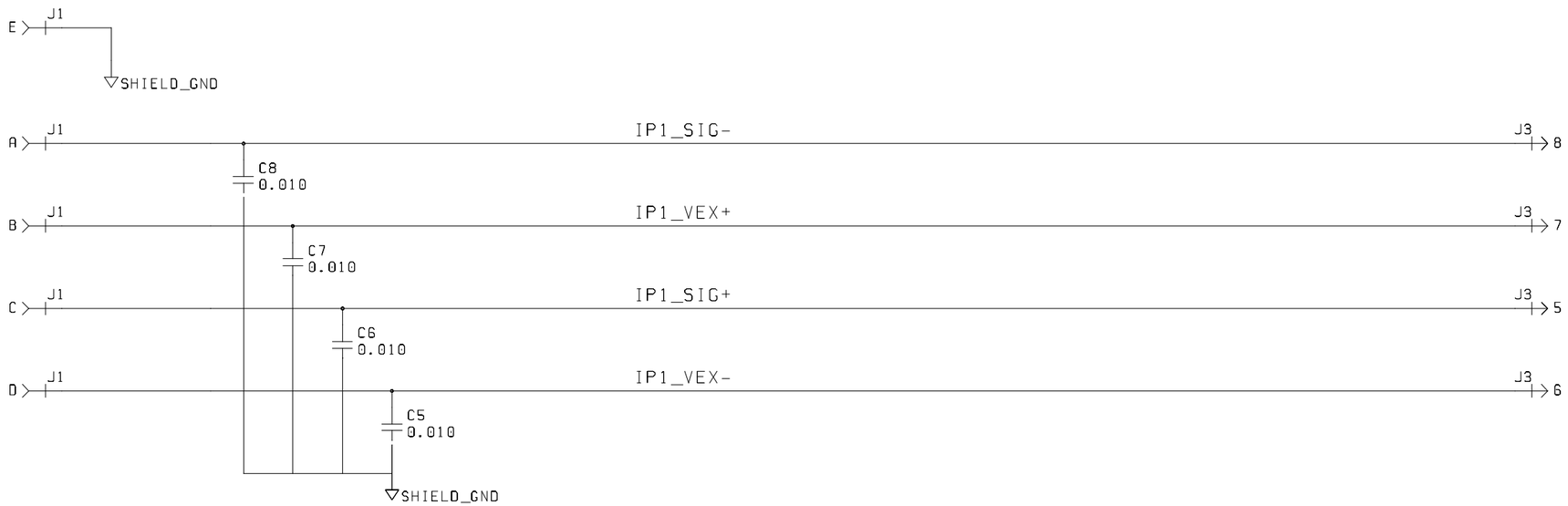
3 - PIN NUMBER 1 IS SHOWN AS SQUARE PAD FOR CONNECTORS.

6 - CRIMP BARREL OF SOCKET(SEQ NO.2) CONTACT TERMINAL WITH AMP TOOL TOOL 90277-1 OR EQUIVALENT TO APPROXIMATELY 0.125 DIAMETER, PRIOR TO PIN INSERTION INTO CONNECTOR ENSURE CONTACT PINS LOCK IN CONNECTOR PRIOR TO SOLDERING TO FLEX ASSEMBLY.

7 - SLIDE FERRITE CORE (SEQ. NO. 3) ONTO CABLE AS SHOWN. SECURE FERRITE WITH 3M 2216 B/A GRAY EPOXY ADHESIVE OR EQUIVALENT.

8 - MAXIMUM LEAD PROTRUSION LESS THAN 0.070.

FO-6D. IP Flex PWA 313-104

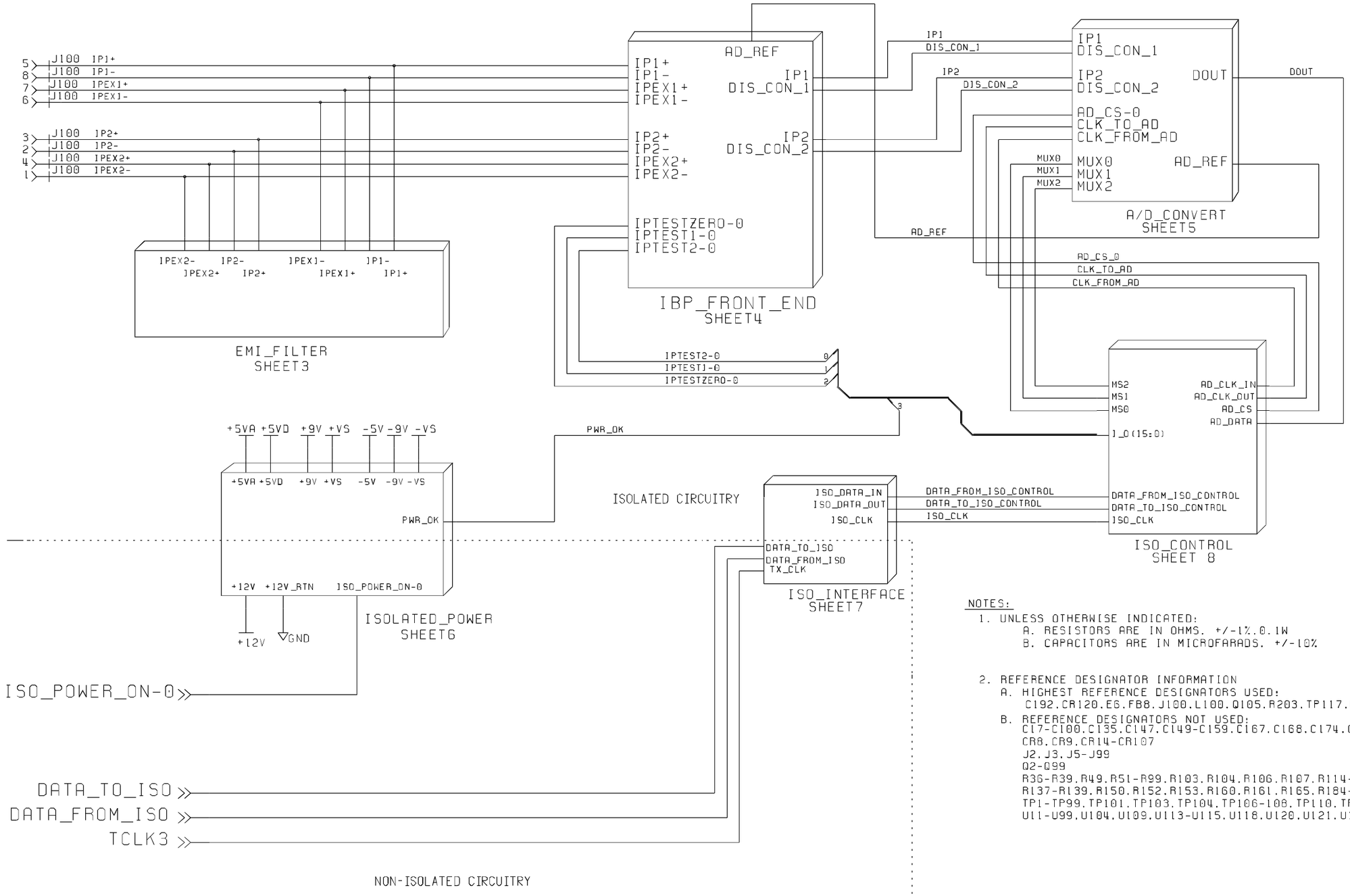


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C8, J3, E1
   B. REFERENCE DESIGNATORS NOT USED:
      NONE

SC313-104 A
IP Flex PWA Schematic (1 of 1)

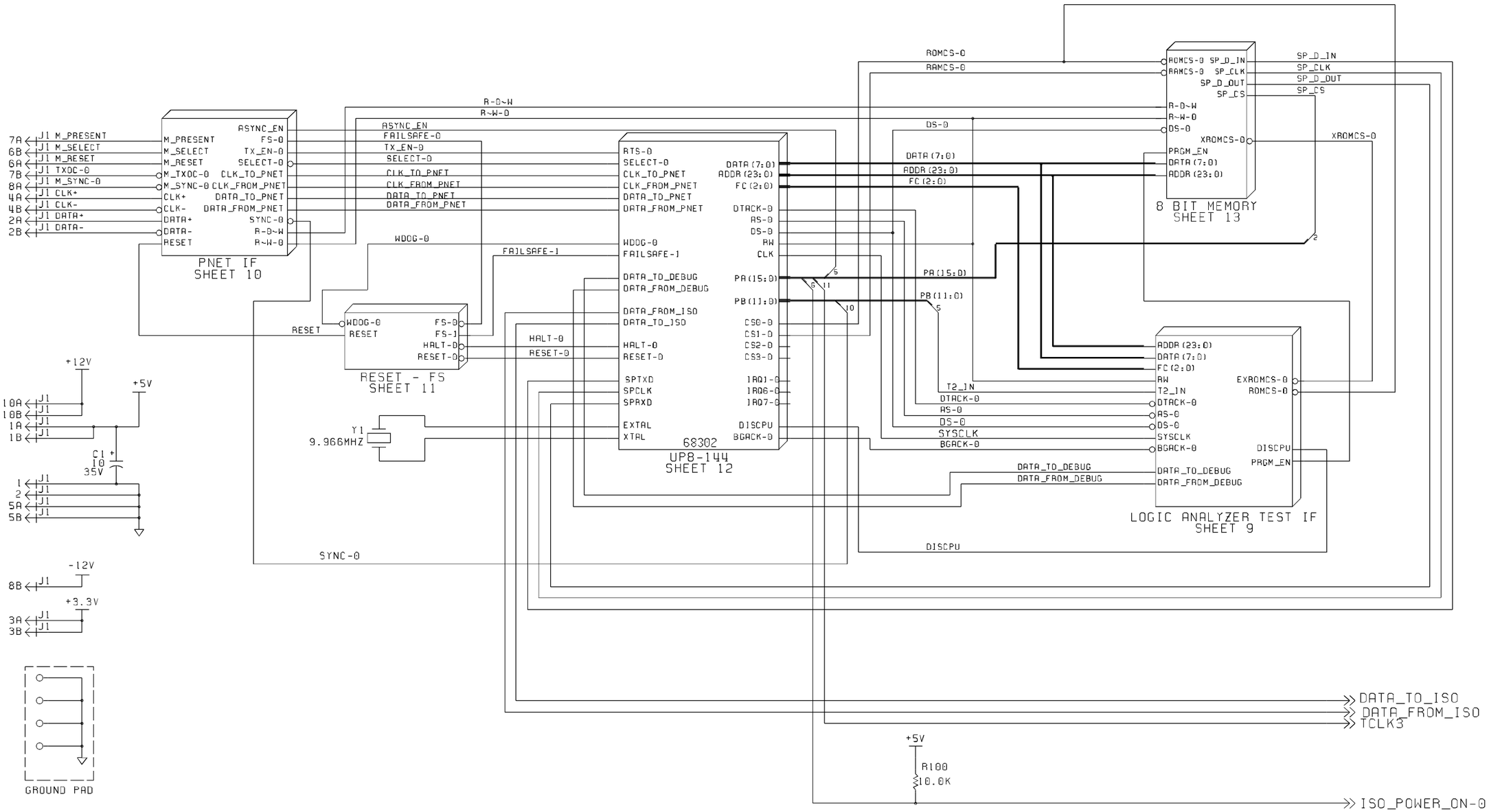


NOTES:

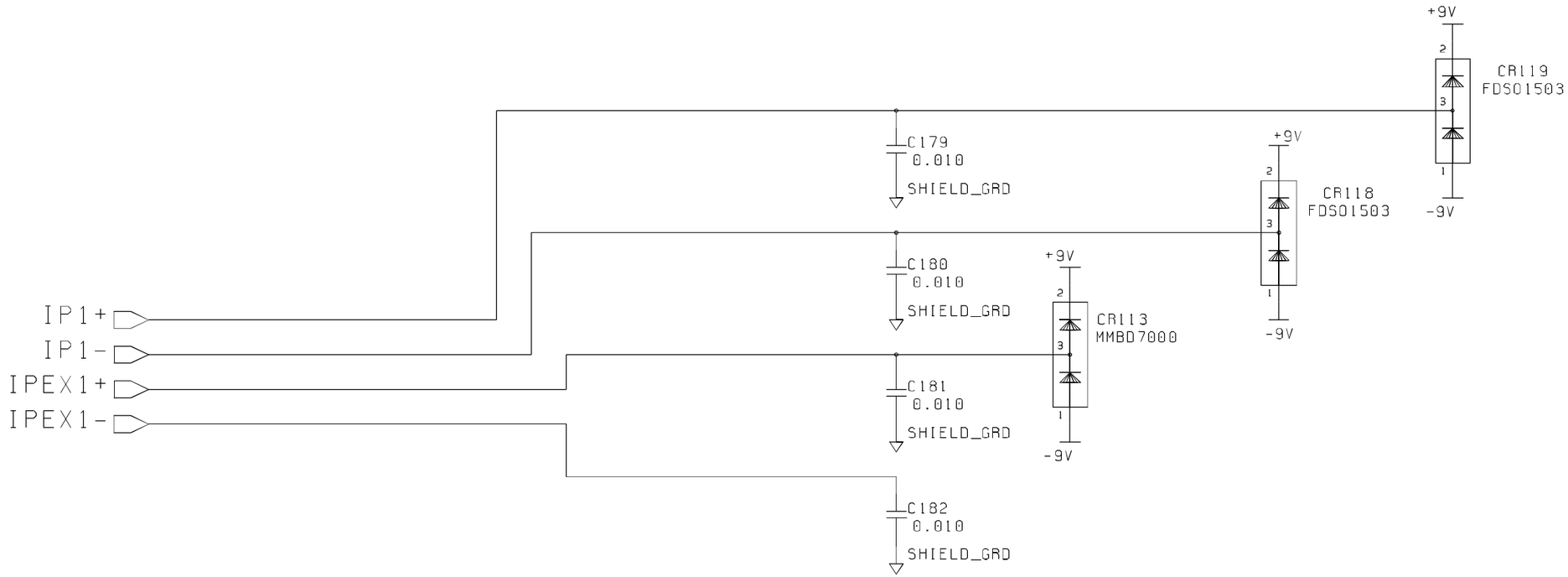
1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS. +/-1%.0.1W
   B. CAPACITORS ARE IN MICROFARADS. +/-10%

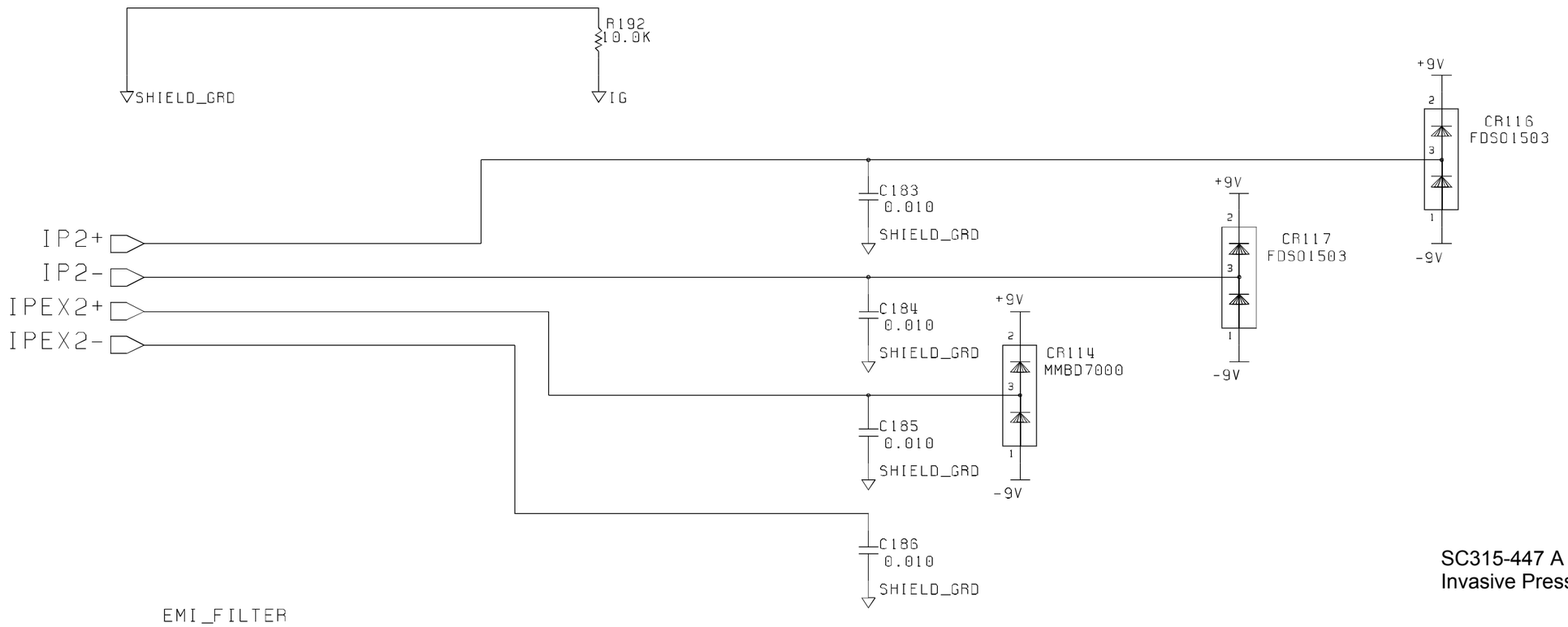
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C192.CR120.E6.FB8.J100.L100.Q105.R203.TP117.U135.Y1
   B. REFERENCE DESIGNATORS NOT USED:
      C17-C100.C135.C147.C149-C159.C167.C168.C174.C175.C177
      CR8.CR9.CR14-CR107
      J2.J3.J5-J99
      Q2-Q99
      R36-R39.R49.R51-R99.R103.R104.R106.R107.R114-R117.
      R137-R139.R150.R152.R153.R160.R161.R165.R184-R186.R196.
      TP1-TP99.TP101.TP103.TP104.TP106-108.TP110.TP113.
      U11-U99.U104.U109.U113-U115.U118.U120.U121.U125-U133

SC315-447 A
Invasive Pressure PWA Schematic (1 of 13)

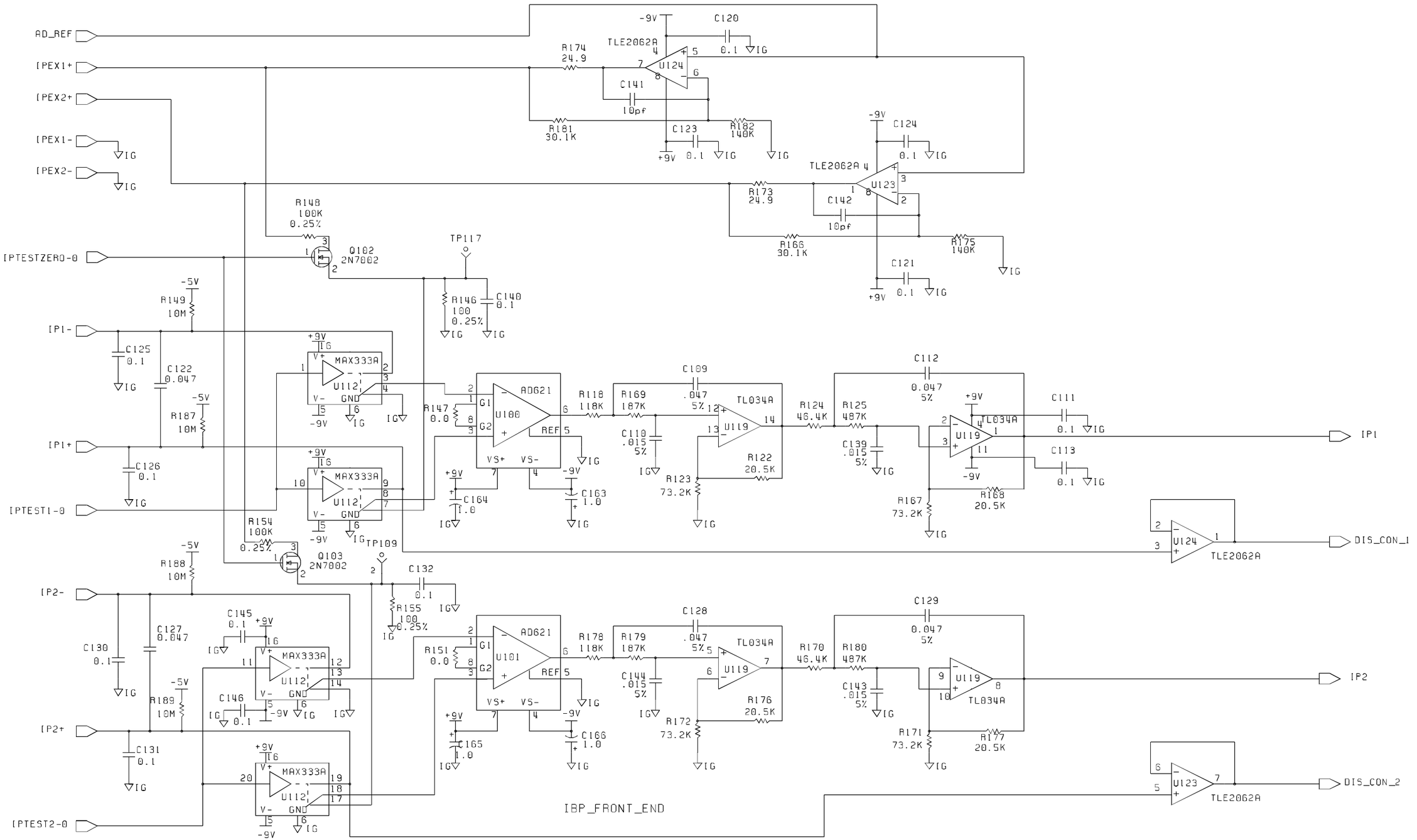


SC315-447 A
Invasive Pressure PWA Schematic (2 of 13)

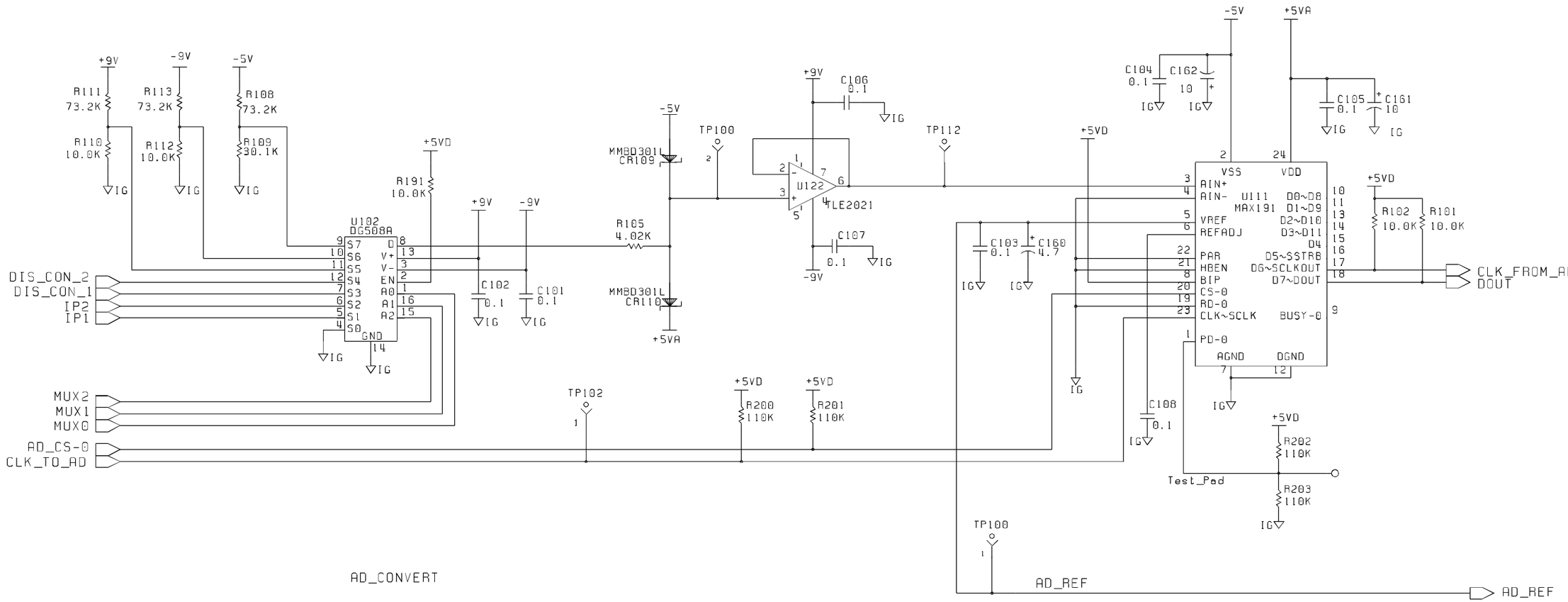




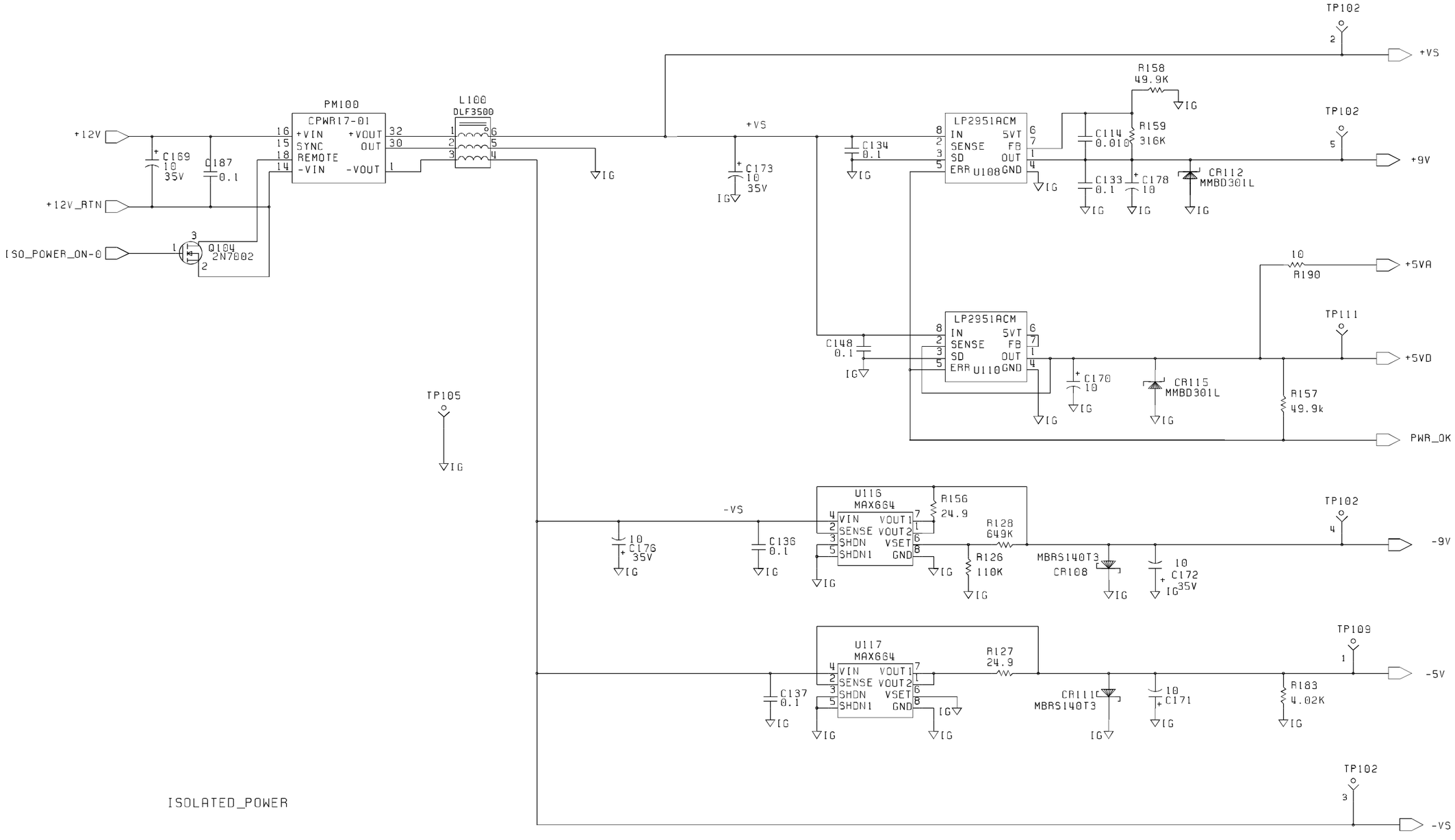
SC315-447 A
Invasive Pressure PWA Schematic (3 of 13)



SC315-447 A
Invasive Pressure PWA Schematic (4 of 13)

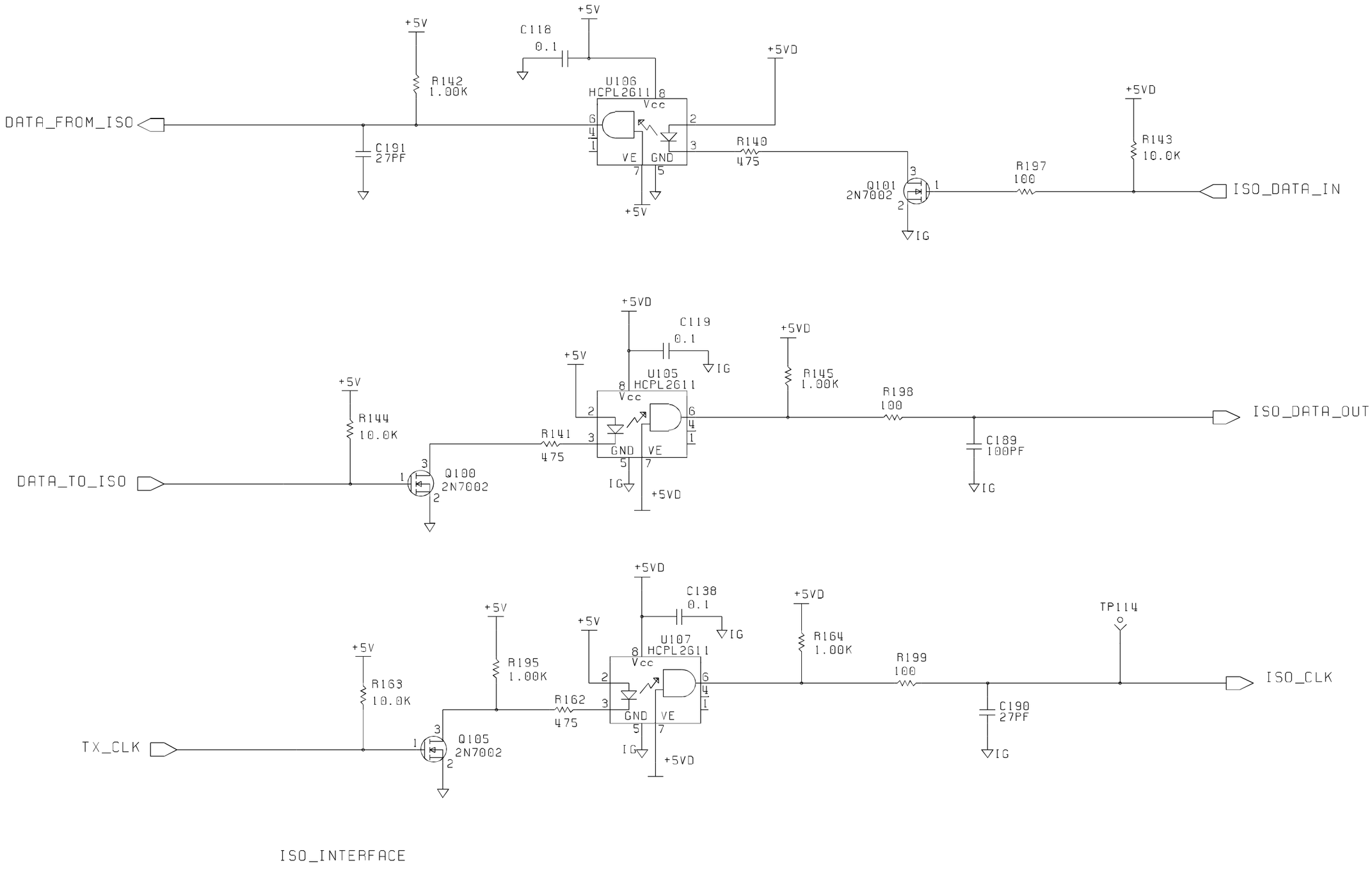


SC315-447 A
Invasive Pressure PWA Schematic (5 of 13)



ISOLATED_POWER

SC315-447 A
Invasive Pressure PWA Schematic (6 of 13)



ISO_INTERFACE

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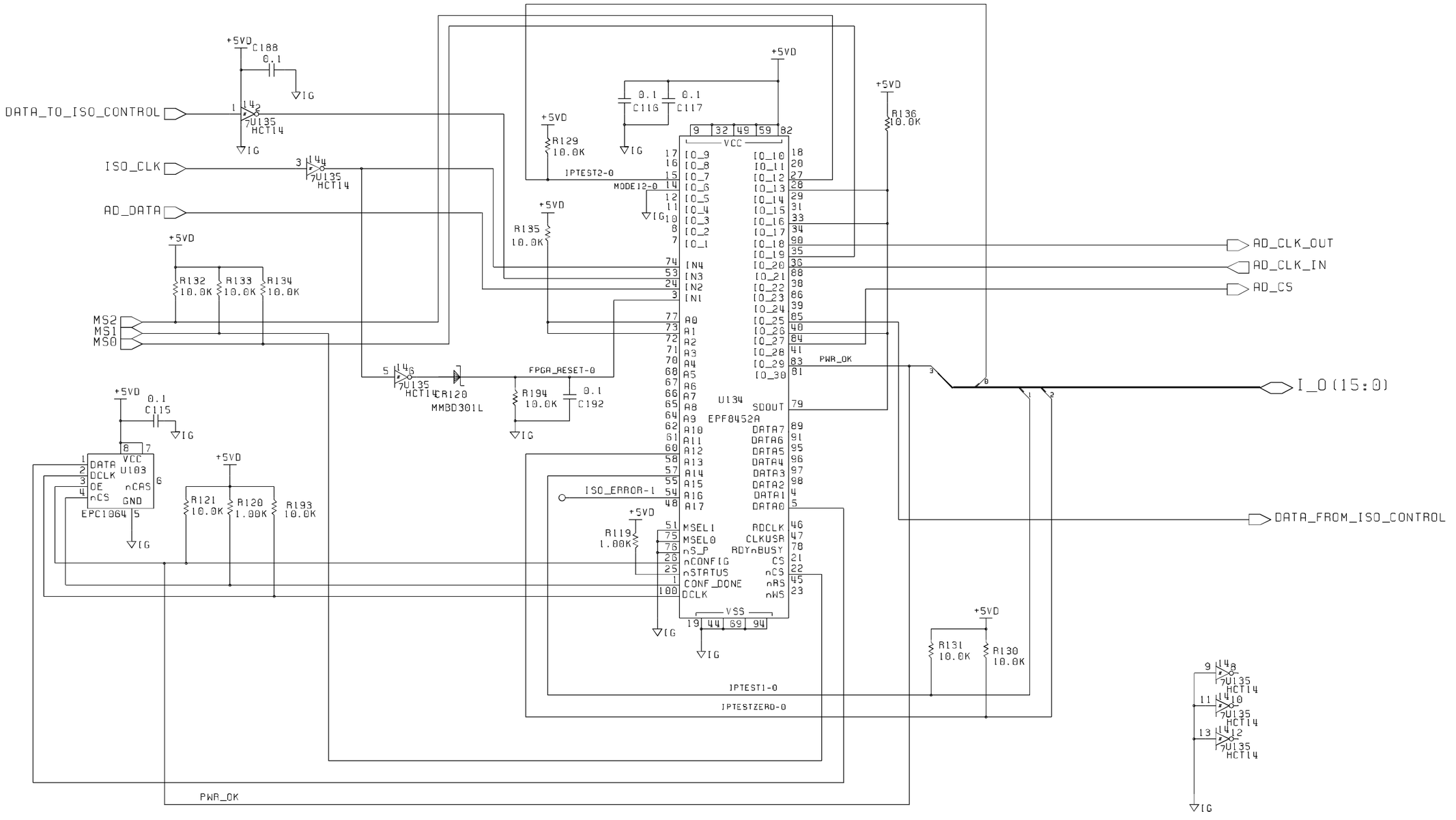
Invasive Pressure PWA Schematic (7 of 13)



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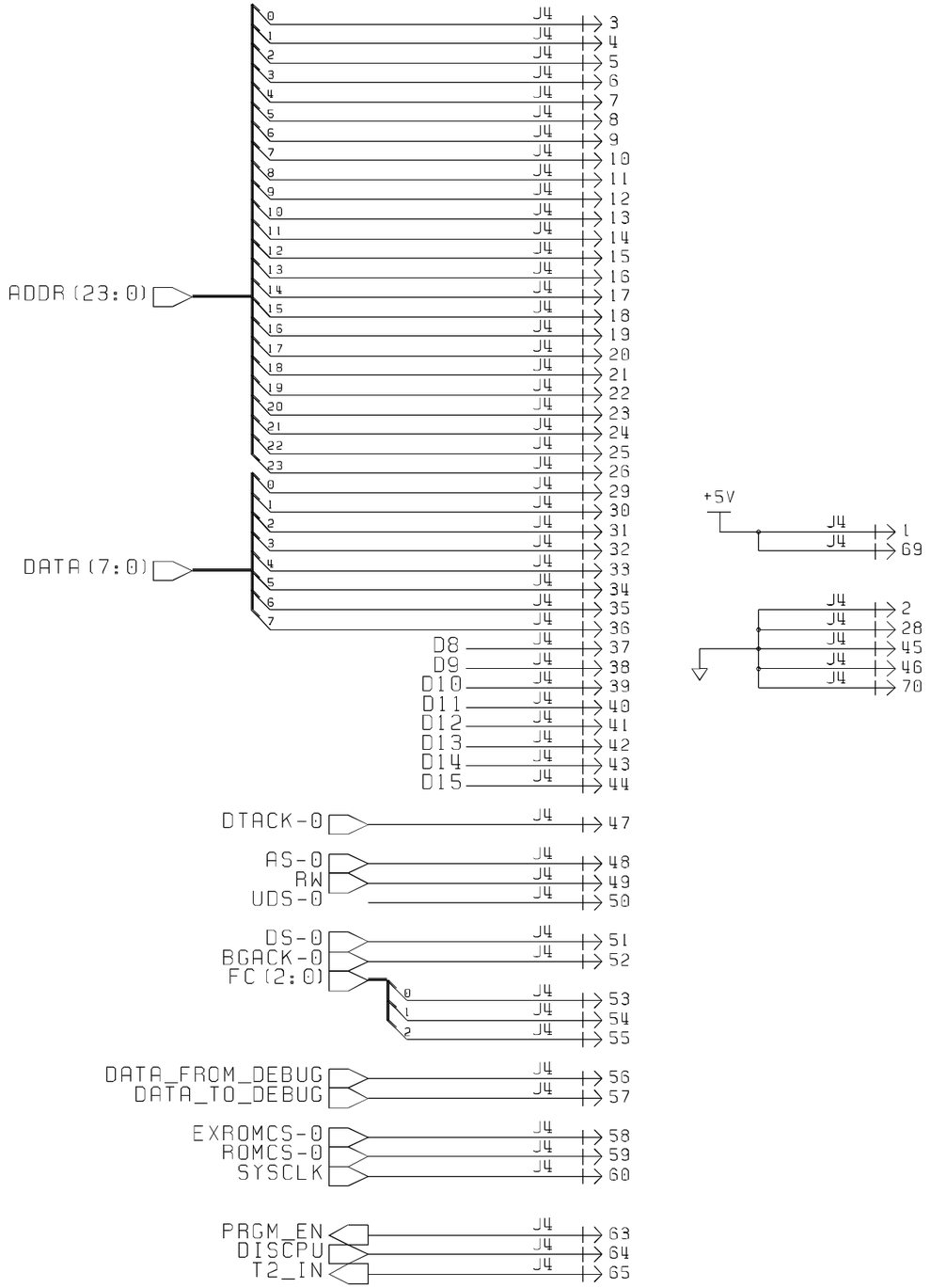
Invasive Pressure PWA Schematic (8 of 13)



LOGIC ANALYZER TEST IF

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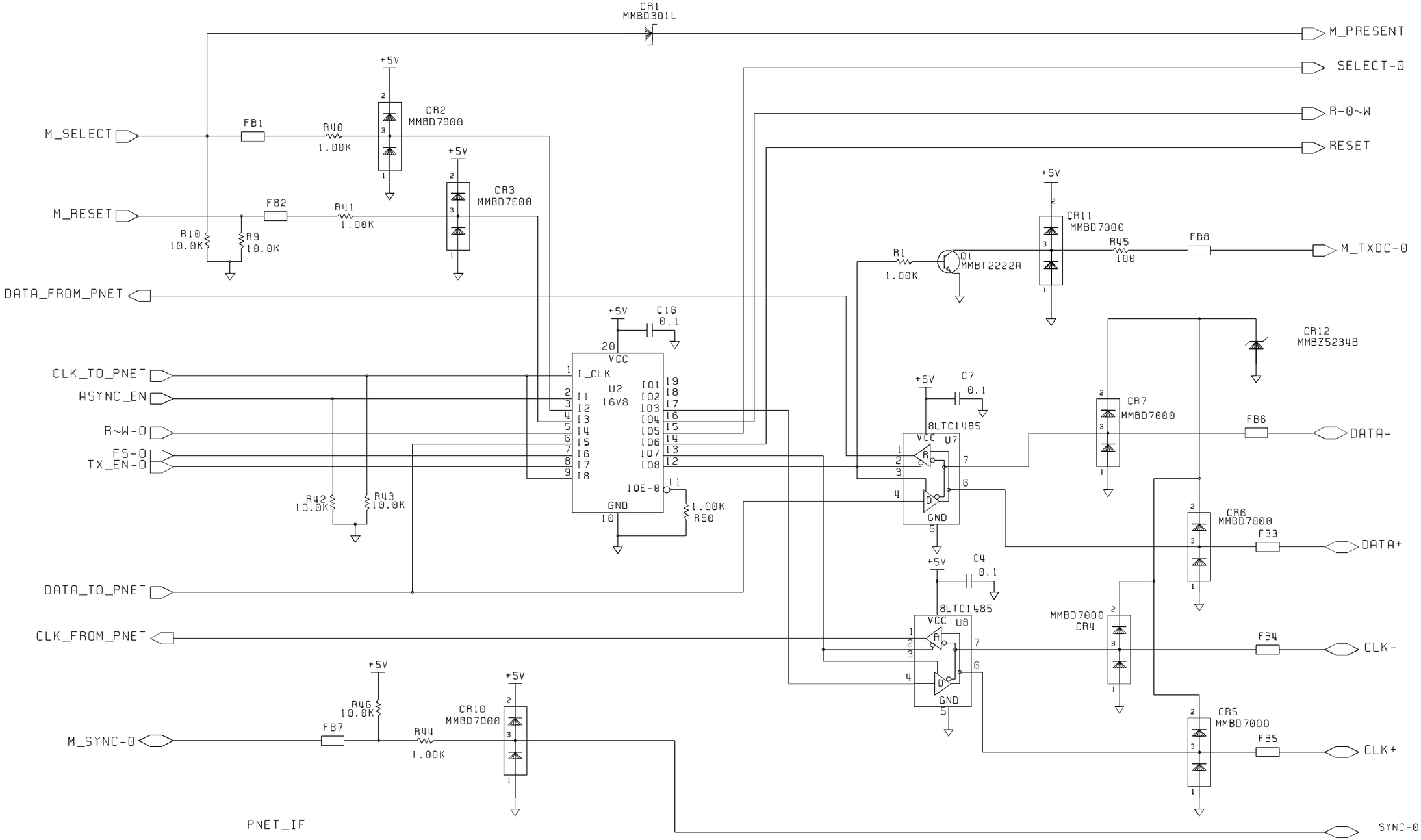
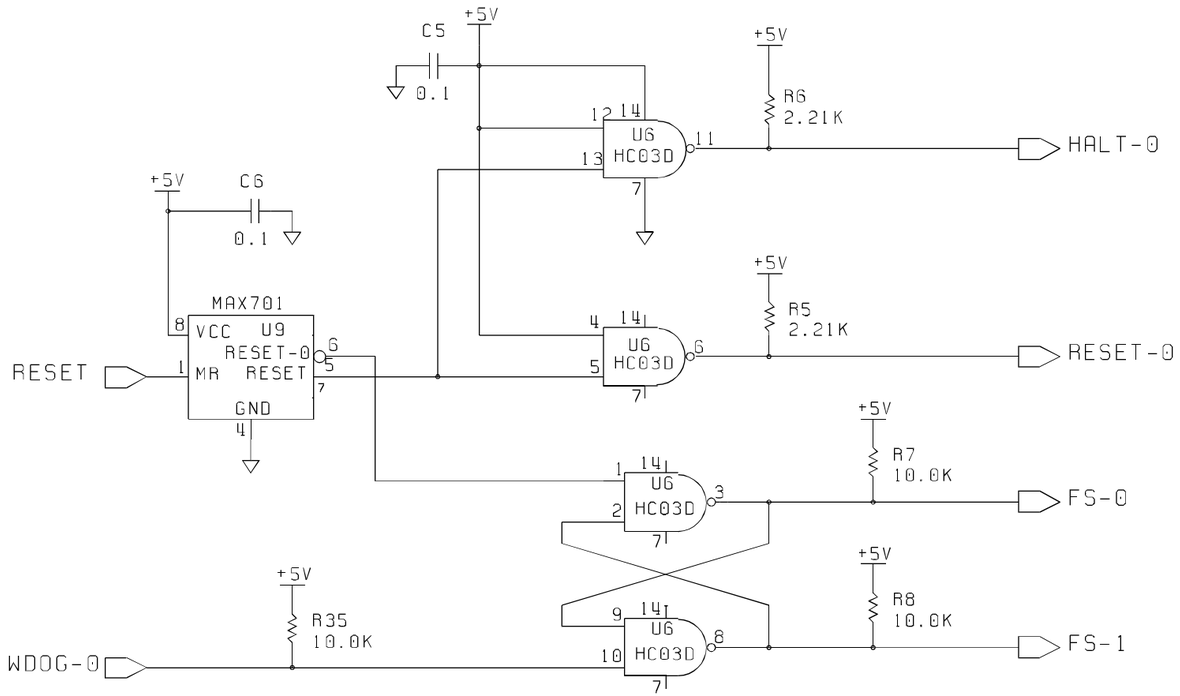
Invasive Pressure PWA Schematic (9 of 13)



SC315-447 A
Invasive Pressure PWA Schematic (10 of 13)



RESET - FS

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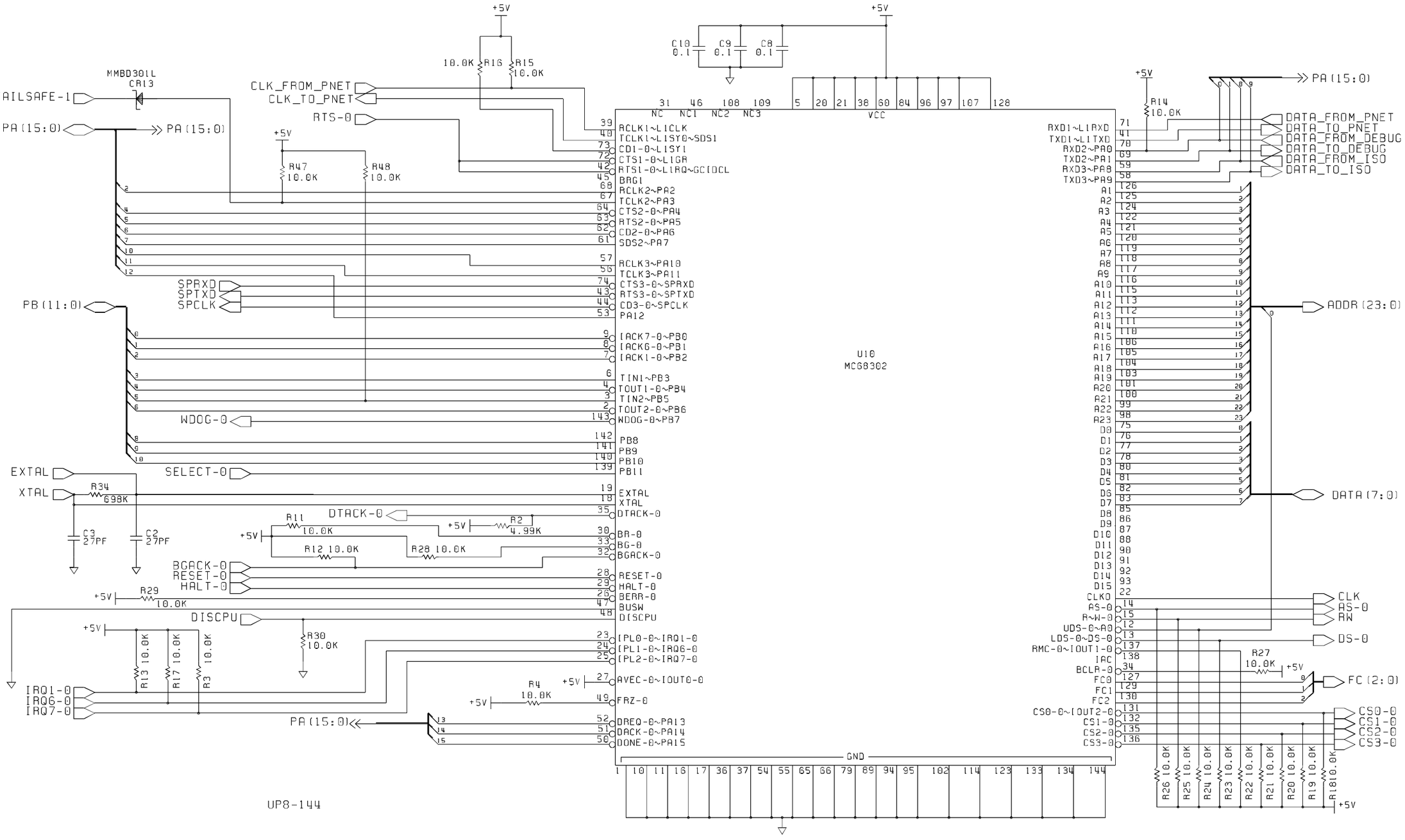
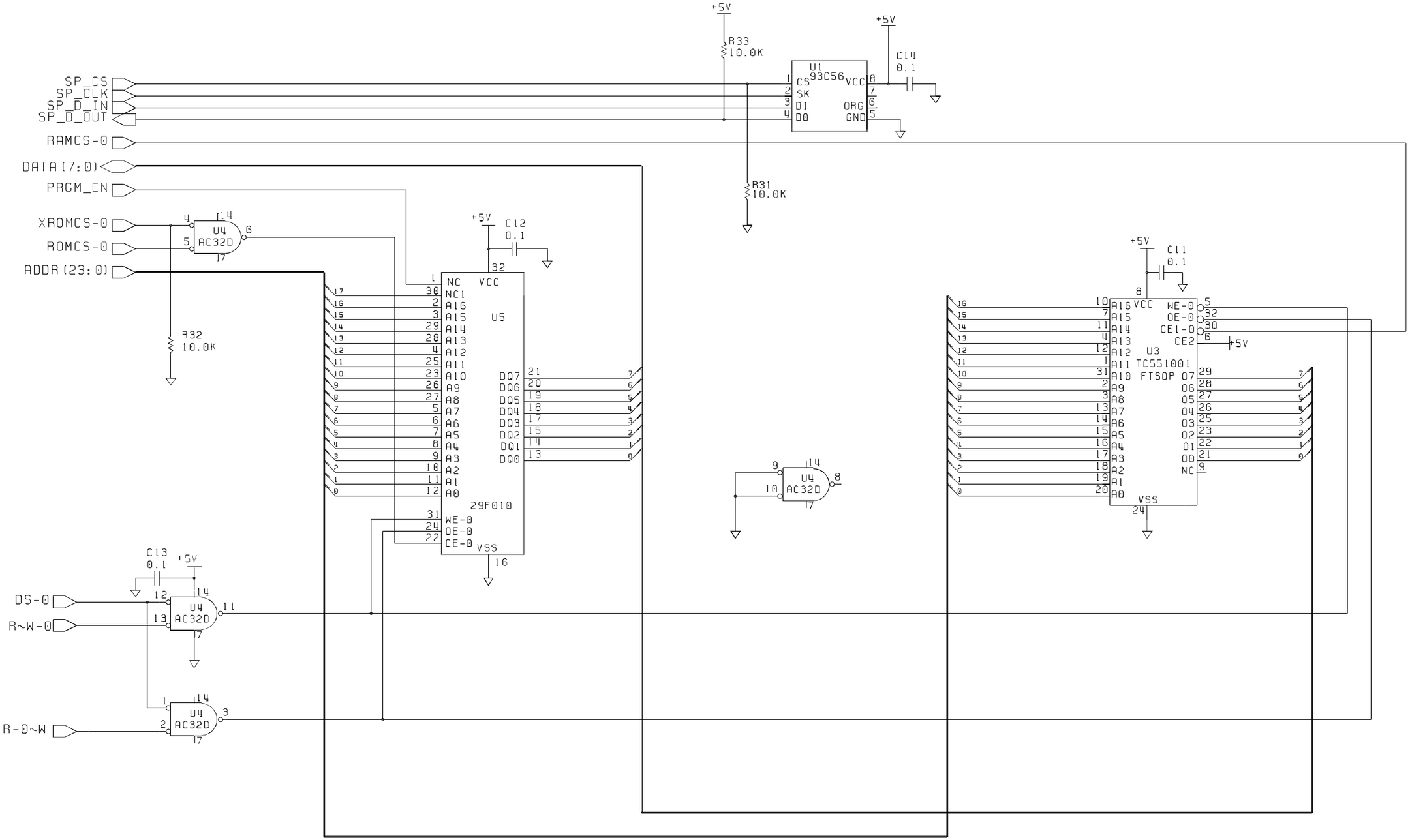
Invasive Pressure PWA Schematic (11 of 13)



SC315-447 A
Invasive Pressure PWA Schematic (12 of 13)



8 BIT MEMORY

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Invasive Pressure PWA Schematic (13 of 13)