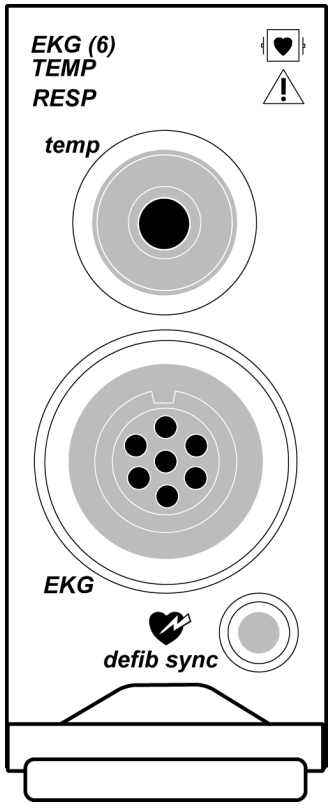
ECG MODULE

INTRODUCTION

This area contains component information about the ECG Module (also referred to as the EKG Module). The singlewide module provides electrocardiographic waveforms in either 3-electrode (Model 7322) or 6-electrode (Model 7324) configurations. The 3-electrode configuration derives waveforms for leads I, II, or III. It includes a waveform cascade feature and can display one waveform as the primary lead. The 6-electrode configuration derives waveforms for leads I, II, III, AVR, AVL, AVF, VA, and VB.



When 4 electrodes are connected to the patient, waveforms I, II, III, AVR, AVL, and AVF are available simultaneously to view and/or to record. When 5 electrodes are connected to the patient, waveforms I, II, III, AVR, AVL, AVF, and a single V lead (chest lead) are available simultaneously to view (maximum of 6 to display) and/or to record. When 6 electrodes are connected to the patient, waveforms I, II, III, AVR, AVL, AVF, and two V leads (chest leads) are available simultaneously to view (maximum of 6 to display) and/or to record.

Breath rate is calculated by measuring the thoracic impedance between two electrodes. As the patient breathes, the movement of the chest changes the measured impedance to produce the respiration rate.

Heart rate values are also calculated as straight or weighted averages over the previous 5 or 10 seconds.

The temperature port of the module allows continuous monitoring of patient temperature using a YSI temperature probe.

PHYSICAL DESCRIPTION

As shown in FO-8B, the module consists of the analog PWA, ECG/temp flex assembly, digital PWA, defib sync flex assembly, card guides, and an enclosure, including front and rear face plates and other metallic hardware. The enclosure and front and rear face plates are grounded metal. The front and rear panels are held in place by long bolts, running from end to end. Insulating guides hold the circuit boards into position in the enclosure, and provide insulation from the enclosure bolts. Sidewall insulators, necessary to maintain patient safety requirements, insulate the module wall.

Front panel connections include a _” stereo jack for YSI 400 Series temperature probes, an ECG connector compatible with the recommended ECG cables, and a 3.5 mm stereo jack connector used for defib sync.

FUNCTIONAL PRINCIPLES OF OPERATION

A functional block diagram of the ECG Module is shown in FO-8A. The diagram is divided into isolated circuitry and non-isolated circuitry. The isolated circuitry includes the ECG flex connector PWA, and either the 3-lead ECG Analog PWA 315-547 (Model 7322) or the 6-lead ECG Analog PWA 315-548 (Model 7324). The isolated (ISO) interface and DC-to-DC converter isolate this circuitry from the non-isolated core logic.

The core logic provides communication between the Module and the Monitor through the PNet synchronous serial interface. It also controls data acquisition and data processing functions for the ECG monitoring channel.

Isolated Circuits

Isolated circuits are shown in the top half of FO-8A, sheets 1 and 2. ECG data is filtered by ECG front end and amplified by differential amplifiers to provide four outputs (ECG1 through ECG4) shown on sheet 1. These ECG signals are filtered by bandpass filters and applied to the multiplexer.

The ISO control and power block serially reads ECG data back to the CPU through the isolated interface. An asynchronous communication channel between the CPU and the ISO control is implemented with a UART. Commands are decoded with control converter U10, which sets the state of multiplexers and switches in the isolated circuitry.

Temperature sensor circuits provide an excitation to the YSI thermistors through a precision resistor bridge. These signals are filtered and amplified and sent to the A/D converter. Temperature is then derived ratiometrically from these signals.

The isolated interface shown on sheet 2 provides an isolated asynchronous serial communication channel between the non-isolated core logic CPU and the ECG isolated front end.

Respiration circuits provide an AC excitation signal through two electrodes. The signal is modulated by thoracic movement during normal breathing. The signal is then demodulated, amplified, and filtered, and sent to the A/D converter, and breath rate is derived.

The isolated power block, consisting of isolated +VAI (+8V nominally), -VAI (-8V nominally), +5VI, -5VI, and +5VID power supplies, provides isolated power to the ECG Module and the sensor connected circuitry.

Non-Isolated Circuits

Non-isolated circuits are shown in the bottom left of FO-8A, sheet 1 and the bottom half of sheet 2. Functional blocks shown on sheet 2 include the PNet interface, DC-DC converter, ISO power control, reset/failsafe, 68302 CPU, 256Kx16 data memory, 256Kx16 program memory, the model and serial number EEPROM, and logic analyzer/test interface.

Power (+12V and +5V), is received through J1. The +12V is applied to the DC-DC converter, which powers the isolated circuitry. ISO power control does not allow the DC-DC converter to power-on until after the CPU is reset and shuts down the DC-DC converter if a failsafe condition occurs.

The Module will not be damaged when plugged into a live slot. Core logic power inputs to a Module are limited to a peak inrush current during hot-plugging. Within 2 seconds the Module will respond to identification and wake up in a minimized power state until registered with the system.

The PNet interface allows asynchronous and synchronous data transfer between the core logic and the external devices. Synchronous operation is always used in MPS systems. Asynchronous operation is for test and development only. The reset/failsafe logic provides power-on reset, processor reset and halt, and failsafes if a problem occurs with the microprocessor. The microprocessor controls and transfers data within the core logic. The program memory is a FLASH device that can be loaded with program information from the PNET interface or the logic analyzer interface. Data memory temporarily stores status and monitoring data for processing.

COMPONENT PRINCIPLES OF OPERATION

Schematic diagrams SC313-108, SC313-109, SC315-546, and SC315-548 are here. The first sheet of the SC315-546 schematic shows an overall block diagram of the ECG Digital PWA. The first sheet of the SC315-548 schematic shows an overall block diagram of the ECG Analog PWA.

Isolated Power Block

The isolated power block is shown on sheets 8 and 9 of ECG digital PWA schematic 315-546. Power converter PM1 converts non-isolated +12V to isolated +VS and -VS. This power is isolated for patient safety requirements. U101, U102, and U103 on the digital PWA are the opto-couplers that provide isolation for communications data and the clock. PM1 is controlled by ISO_POWER_ON from the CPU via Q103. This signal disables PM1 if a failsafe condition occurs. The +VS and -VS (unregulated) voltages from PM1 are filtered by L100 and applied to regulators U105, U106, U107, U108, and U111.

These regulators supply isolated power to ECG analog PWA 315-548. The voltages are:

+5 VID for digital circuits
+5 VI for analog circuits
-5 VI, +VAI (+8 VDC), -VAI (-8 VDC)

Error outputs from positive regulators U105, U106, and U111 are OR'ed together to provide PWR_OK. If a power supply output drops 5% below the regulated output, PWR_OK goes low, which causes the CPU to shut down the isolated supply.

Isolated Control Circuits

The isolated control circuits are shown on sheets 14 and 15 of ECG analog PWA schematic 315-548. Field programmable gate array (FPGA) U103 contains the state machine, which provides an interface between the isolated analog circuitry and the main CPU on the non-isolated circuitry of digital PWA 315-546. Communication is achieved through a UART, which provides a full duplex asynchronous serial communication channel between the CPU and the isolated circuitry. On power up, the non-volatile program data for the FPGA is loaded from serial EPROM U105 into U103. After several hundred milliseconds, the FPGA is configured and ready to run. CLOCK for the state machine is a 5.9 MHz signal provided from the CPU via opto-couplers located on the digital PWA.

Commands are sent serially (via opto coupler for isolation) through DATA_IN. Data is sent back to the CPU by DATA_OUT and is also optically isolated (on the digital PWA).

The state machine responds to commands to perform A/D conversions or to change the states of multiplexers or switches. It provides the control for the serial A/D interface, a 1.5 MHz clock to the A/D (ADC_SCLK), and proper control signals AD_CNVST to initiate a conversion.

Digital signals are also read back on command to provide the CPU with status information. Board configuration (single lead, part number 315-547 or multi lead, part number 315-548) is determined by the PWA_CFG bits located on sheet 15 of analog PWA schematic 315-548, and provided to the CPU on command. Pacer detection status is another status that the CPU monitors.

The state machine also derives the respiration clock signals (RESP_CLK and DM_CLOCK) and switched capacitor filter clock (LPF_CLK) as divided down versions of the main 5.9 MHz clock.

ECG/RESP Inputs

Three lead (3-electrode) and six lead (6-electrode) cables are available for ECG. The 3-electrode cable provides a single lead configuation with Leads I, II or III available. The 6-electrode cable provides multiple leads with up to 8 leads available: I, II, III, AVR, AVL, AVF, VA and VB. The 6-electrode cable may be used with 3, 4 , 5, or 6 electrodes. (Refer to the EKG section of the Operation Manual for a description of which leads are available with the number of electrodes connected.) In single lead (3-electrode cable), signals RA, LL, and LA are used. In multi lead (6-electrode cable), signals RA, LL, LA, RL, C1, and C2 are used.

The cables recommended by JJMI are shielded and provide 1k ohm series (safety) resistors internal to the cable which is part of the current limiting defibrillator protection circuitry.

The signals are input to the flex PWA 313-108. Gas surge arrestors located on the PWA provide lead-to-lead defibrillator protection. In addition, a passive R/C network located on this PWA provides the first stage of high frequency filtering for EMC and ESU interference rejection.

The signals are then applied to analog PWA (part number 315-548 for multi lead, or part number 315-547 for single lead) via J101.

RESP Input

The RESP input is shown on sheet 10 of ECG analog PWA schematic 315-548. Of the ECG signals, RA, LA, and LL are also used by the respiration circuit. Respiration is achieved by coupling an excitation signal (61.5 kHz, well outside the bandwidth of normal ECG signals) onto two of these signals. When respiration is using Lead I, the excitation is coupled onto RA and LA. When respiration is in Lead II, the signal is coupled onto RA and LL.

The excitation signal is coupled onto the EKG leads through coupling capacitors C179, C180, and C200. The coupling capacitors isolate the ECG signal from being loaded down by the respiration circuit. Photo relay U121 determines which lead is selected. T100 provides a differential excitation source. CR108, CR112, and CR113 provide clamping protection for transients.

ECG_RESP_INPUT

The ECG_RESP_INPUT is shown on sheet 2 of ECG analog PWA schematic 315-548. The ECG signals are passively filtered by R/C network R314, R315, R316, R372, R373, R374, C201, C257, C258, C259, C221, and C222 at 5 kHz for interference rejection of high frequency noise and ESU. Also, the excitation signal for respiration signal is attenuated and kept out of the ECG channel circuitry and pace detection circuitry. Protection diodes CR114-116 and CR125-127 protect against transients during both defibrillation and ESU events. R368 through R371 and R310, R212, and R213 are light pullup resistors which limit DC current through the electrodes and are used to determine when an electrode has become disconnected from the patient.

ECG Front End

The ECG front end is shown on sheet 3 of ECG analog PWA schematic 315-548. The filtered ECG signals LA_FLT, RA_FLT, LL_FLT, RL_FLT, C1_FLT and C2_FLT are buffered at U122 and U138 and then multiplexed at U132 to be read by the A/D. These signals are used to help determine which electrodes are connected to the patient. These signals (or sums of these signals in the case of chest leads) are also differentially applied to the instrumentation amplifiers U119, U126, U133, and U134 with gains of X10, and create the first stage of the four ECG channels.

The signals also generate a common mode nulling signal by summing all the necessary leads at U127 and U136 for a given mode, inverting the sum, and amplifying and applying the null signal at the selected reference or driven signal at U137. The signals selected at U127 to generate the common nulling signal depend on which electrodes are available and which mode the module is in - single lead or multi lead.

Additionally, U128 provides the means to make ECG instrumentation amplifier U119 selectable between LEAD I, II, or III. U135 and U122-8 provide the means for applying various test signals to the ECG channels and the pacer detection circuit. Signals at U127-5,6,7 are also used in various test modes using the Service Mode facility.

Pace Detector

The pace detector and filter are shown on sheets 4 and 9 of ECG analog PWA schematic 315-548. Pacer signals present on ECG waveforms are detected by the pacer detection circuitry. Any of the 4 ECG channels (outputs of the instrumentation amps) may be used to detect pacers. The channel is selected at U125, sheet 4. When a paced ECG waveform is present and pace detection is enabled, the pace detector circuit will detect the presence of a pacer pulse and blank the ECG channels during the pacer pulse to suppress pacer spikes in the ECG channels.

The detector on sheet 9 consists of a high gain bandpass filter at U113 (200Hz to 5kHz) which rejects both respiration excitation remnants, and 60 Hz and is sensitive mainly to waveforms with pacer signals present. When a pacer pulse is present, the output goes above or below the limits set by the window comparator at U108 and causes PD_TRIGGER to go true to indicate the presence of a pacer.

When enabled, the detection of a pacer causes the ECG channels to be blanked. This is achieved by the opening of the channels at U124 and the channel hold capacitors, C189,188, 165, 194 (sheets 5 through 8). The channels are blanked during the entire duration of a pacer pulse.

ECG Channel Filters

ECG channel filters are shown on sheets 5 through 8 of analog PWA schematic 315-548. The circuits for the ECG bandpass filters are duplicated for the four channels on sheets 5 through 8. The description of channel 1 (on sheet 5) is similar for the other three channels.

The bandpass filtering is achieved mainly through 8-pole switched capacitor filter U110, which has a cutoff at 115 Hz and through integrator circuit U111-12,13,14, which strips off the DC component of the ECG waveform. This is the MAIN anti-aliasing filter for the ECG channels. (Sampling frequency in normal use is 1200 Hz.) The cutoff frequency of the swithed capacitor filter is determined solely from its input clock frequency (LPF_CLK, 11.5kHz). This clock signal divided by 100 gives the 115 Hz lowpass response. The resulting frequency response of the entire bandpass filter section is approximately 0.05-115 Hz with a gain of 12. With the earlier instrumentation amplifier stage this give an approximate ECG channel gain of 120. The filtering stage prior to the switched capacitor filter at U111 provides low pass filtering and anti-aliasing prior to the switched capacitor filter and has an approximate 3dB point at 1kHz and a gain of 5. The filtering stage after the switched capacitor filter at U111-8,9,10 also has a 1kHz 3dB point for eliminating any clock noise from the previous filter stage and has gain of 2.4. Thus the X5 and X2.4 give the gain of 12 in this stage.

Q103 and R218 provide a means to quickly charge the integrator stage (0.05 Hz high pass stage) to reestablish a new baseline during lead switching or new lead attachment. The output of the channel at ECG1_OUT is then routed to main mux U102 to be used by the A/D converter.

Respiration and Filters

The ECG respiration circuits and filters are shown on sheets 10 and 11 of ECG analog PWA schematic 315-548. The respiration clock RESP_CLK controls the analog switch U114 providing an excitation signal of 61.5kHz from quiet reference U120 to buffer U115, where it is filtered and then drives transformer T100 where the signal driven differentially on the two selected respiration leads RA_RESP and LA_RESP or LL_RESP. RESP_LEAD_SEL selects the respiration leads through U121 (LEAD I or LEAD II). DM_CLOCK, slightly off phase from RESP_CLK, is used to provide a synchronous demodulator with U114 and U115. The demodulator rectifies the waveform and the signal is then filtered through a bandpass filter (sheet 11) with a frequency response of 0.1-5 Hz.

As the patient's chest rises and falls due to breathing, the impedance of the chest typically changes by several ohms. The excitation is a constant current source so a change in impedance causes a change in amplitude of the voltage which is sensed at T100-1. Essentially the carrier (excitation signal) is slowly AM modulated by thoracic movement. The demodulation allows the slow respiration signal to be detected. The filter eliminates the 61.5kHz carrier signal and leaves the respiration signal. The filter is implemented in several stages at U109 with a total gain of x600. RESP_OUT then goes to the main mux where it is read through the A/D converter. Similar to the ECG channel, Q102 allows the integrator to quickly charge to a new baseline during lead switching and new lead attachment.

RESP_BL_OUT (respiration baseline) on sheet 10 is a signal derived from the diode-rectified carrier (asynchronous demodulation) signal at CR111. The impedance of the chest movement during breathing is a small dynamic change of several ohms riding on top of a relatively large impedance or baseline (typically 100-2000 ohms). The RESP_BL_OUT gives an indication of this baseline impedance. If this signal becomes too large, it is an indication that a respiration electrode has fallen off or is dried out and has become too large of an impedance.

U114-2,9 and R152,C139, R196 and R236 and Q104 provide the means to test the respiration circuitry. Using the Service Mode facility, a test can be commanded to run which uses these components to stimulate the respiration circuit with a dynamic impedance (approximately 10 ohms) that is square wave in nature.

Temperature Circuits

The temperature circuits are shown on sheet 12 of ECG analog PWA schematic 315-548. The temperature circuit is used to monitor YSI 400 series temperature probes. It works by determining the ratio of the YSI probe resistance to that of a precision reference resistor. This is accomplished through a voltage divider circuit. An excitation voltage (TEMP_EXC, 0.385 volts nominally) at U107-1, is generated across the reference resistor (R154) and the probe thermistor (in series with the reference resistor). The excitation voltage and the voltage across the thermistor are filtered and amplified with a gain of 5.44 at U106, 107 and measured by the A/D converter. The ratio of the reference resistor to the thermistor resistor can be determined from the measured voltages.

Once the resistance of the YSI probe is determined, the temperature is found, by means of a look up table, from the thermistor's electrical resistance versus temperature relationship. The electrical thermistor data is provided by YSI.

Relay K100 allows a test resistor (R153) to be switched in to verify the temperature circuitry. When the relay is de-energized the excitation is applied to the external probe at TEMP_HI. In the energized state the excitation is applied to the test resistor. The voltage at U106-9 at R153 is also monitored to verify the correct operation of the relay contacts.

TEMP_HI and TEMP_RET via J101 reach the front panel of the ECG module at the 1/4" stereo jack by Flex PWA 313-108. This flex circuit contains bypass caps which help filter out high frequency interference in the temperature signal path.

At U106-7,-10,-11,-12, other inputs included are scaled versions of the power supply voltages. The voltages are sent to the A/D converter, and are used to monitor the analog supply voltages. Using the Service Mode facility, the self-test mode can be initiated and resistor values and derived temperatures can be observed.

Multiplexer and A/D Converter

The multiplexer and A/D converter are shown on sheet 13 of ECG analog PWA schematic 315-548. These circuits sample analog ECG data and provide this data serially to the CPU. EMUX, ECG1 through ECG4, TMUX and respiration outputs are applied to analog multiplexer U102. The multiplexer output is selected by MUX (2:0), and the multiplexed output is applied to buffer U100. This signal is clamped at +/- 5VI by CR100. The buffer output is applied to A/D converter U101, which is clocked by ADC_SCLK_0 (1.5 MHz). The digital data (ADC_DATA) is clocked out of the A/D converter serially by ADC_CLK and sent to the CPU. The A/D converter also provides a stable reference voltage (3.0V VREF) for the temperature circuit on the analog PWA.

Defibrillator Synchronization Interface

The defibrillator synchronization interface is a non-isolated signal input/output meant only for connection to another medical device that is compliant with UL 2601/IEC 601-1. Connection to a non-compliant device could result in a safety risk by exceeding current limits.

The defib sync connector provides an analog ECG waveform output. It also accepts a synchronization signal (marker input) from defibrillators that provide this feature. If a synchronization signal is detected a marker is placed on the primary lead waveform displayed by the Monitor. The analog ECG waveform signal is a high level (1V/mV) representation of the primary lead.

The defib sync connector is a three-conductor 3.5 mm stereo jack that mates with a 3.5 mm stereo plug (Shogyo SPY 1011, Shogyo SPY 1012, or equivalent). Cable construction should be shielded, 3 conductor with PVC insulation or equivalent insulating material.

Pin Out:

Tip	Marker input
Ring	ECG analog output
Sleeve	Signal return

ECG Analog output specifications, implemented with 10-bit DAC U104 and filter circuit of U110, on the digital PWA:

Scale Factor	1V/mV
Output Impedance/Short Circuit Protection	1k ohm
Bandwidth	0.5 Hz-100Hz

The sync marker input is compatible with the HP defibrillators. The marker signal is active when the input is driven below ground. A pullup resistor allows this input to be driven by an open collector output. The input must be driven below -1V to be detected as a marker. The input is pulled up to +5V by a 20k ohm resistor. Therefore, the output impedance of the driving device must be such that the input can be driven below -1V.

Marker input specifications, implemented at U100 on the digital PWA:

Input Range	+5V to -12 V
Trip Voltage Range	0V ± 1V
Minimum Marker Pulse Duration	10 ms

Protection diodes clamp any input to +5V on the high side or to -12V on the low side. A 1k series resistor limits current during any over voltage condition.

The stereo jack provides two shunting contacts for sync cable detection. When a plug is inserted, the contacts separate. One of these floating contacts is used to sense a connected plug. CONNECTED-0 indicates to the CPU that a plug has been inserted into the front panel connector.

Isolated Interface

Opto-couplers U101 and U102 shown on sheet 8 of ECG digital PWA schematic 315-546 provide a full duplex, isolated serial channel between the non-isolated core logic and the isolated circuitry. The isolated control block, located on sheet 14 of ECG analog PWA 315-548 receives data through opto-coupler U101 and transmits on U102. Opto-coupler U103 transmits the baud clock, which provides the 5.9 MHz clock (ISO_CLK) to the Isolated Control State Machine. Q100, Q101, and Q102 buffer the signals to the opto-couplers. Q102 is pulled up to +5V to speed up the rising edge of TX_CLK.

Core Logic

The core logic is shown on sheets 2 through 6 and sheet 8 of ECG digital PWA schematic 315-546. The core logic provides communication between the system host and the ECG Module through the PNet synchronous serial interface. The Module is a 16-bit version of the core logic with two 128K x 8 RAM and two 128K x 8 ROM devices. The microprocessor runs at 23.646 MHz.

PNet Interface

The PNet interface, shown on sheet 2 of the schematic, provides the following functions:

- RS485 diffeential drivers (U7 and U8) for serial data and clock,
- Module select and presence detection (U2),
- Module synchronization.

Core signals are received on PNet connector J1 (sheet 1) with the following pin-out:

PIN	NAME	PIN	NAME
1A,1B	+5V	6B	M_SELECT
2A	DATA+	7A	M_PRESENT
2B	DATA-	7B	TXOC-0
3A,3B	+3.3V	8A	M_SYNC-0
4A	CLK+	8B	-12V
4B	CLK-	10A,10B	+12V
5A,5B	GROUND	1,2	GROUND
6A	M_RESET		

The ECG Module is designed to be hot-plugged, or inserted and removed from powered systems. Ground pins 1 and 2 are longer than the other connector pins, thus they make first and break last to protect circuitry. Protective impedance located on the system backplane, in series with the Module's +5V and +12V power, limits inrush current during live insertion. Also series impedance on PNet control lines limits inrush current and protects logic devices from excessive currents during a hot-plug power up.

The PNet protocol defines two modes of operation: synchronous and asynchronous. The normal mode of operation is synchronous, with half duplex transmitted and received data on differential signals DATA+ and DATA-. As shown on sheet 2 of the schematic, the device transmitting the serial data also generates differential clock signals CLK+ and CLK-. Transceiver direction for data and clock are controlled by the 68302 processor-generated TX_EN-0 (low true transmit enable) signal through U2. In the synchronous mode, both data and clock transceivers U7 and U8 are set to receive (i.e., transmit disabled) when fail-safe signal FS-0 is asserted.

The alternate serial mode, full duplex asynchronous, is entered by asserting processor generated control bit ASYCH_EN. This mode transmits data onto the differential signals CLK+ and CLK-, and receives data from the differential signals DATA+ and DATA-. The transmitter in the Module is disabled unless the Module has been commanded to transmit per the PNet protocol. The Module transmitter is immediately disabled after the last character of a transmission has been sent.

The Module select input (M_SELECT, hi true) instructs the Module to respond to identification requests. When both M_SELECT input and M_RESET input (hi true) are asserted, the Module performs a hardware reset.

The Module present output, M_PRESENT is connected to M_SELECT through diode CR1 to allow a means of determining if the Module is plugged into an instrument. When M_SELECT is asserted (pulled hi) M_PRESENT is hi true.

Module transmitter open collector signal TXOC-0 from Q1 signifies the Module transmitter is enabled. Serial data is then transmitted in the synchronous mode.

M_SYNC is used for timing of shorter latency periods than supported by the serial data protocols. A Module only asserts M_SYNC when enabled by the host.

Reset Logic

The reset logic is shown on sheet 3 of the schematic. Reset logic U9 generates a power-on-reset when power is applied. RESET-0 and HALT-0 signals remain low for minimum of 130 msec after all logic voltages are in specification.

External reset, processor reset, and halt signals are low for minimum of 24 clocks when external reset is asserted. Power monitoring, processor reset, and halt signals are low if logic voltages drop below specification. They remain low for minimum of 130 msec after logic voltages return to the specified range.

The reset circuit consisting of U6b and U6d provides open drain outputs to the processor bi-directional reset and halt signals.

Fail-Safe Logic

Fail-safe latch (U6a and U6c) ensures that the Module enters a safe state if the processor fails to operate correctly. The latch is set by a low true output from the processor watchdog timer (WDOG-0). The data transmitter is disabled, isolated power is shut down, and the Module remains in a safe state until the latch is cleared by a power on or external reset.

Microprocessor

The core logic design is based around the 68302 microprocessor (U10) shown on sheet 4 of the schematic. The 68302 combines a 68000 core with a three channel communication processor, and system integration circuits.

The left side of the CPU contains clock interfaces to/from the PNet, port A, and port B to various circuits in the core logic, reset, and halt interface. The IRQ ports are not used. The right side of the CPU contains address lines, data lines, and chip select outputs. The 68302 operates with a statically defined 8-bit wide bus. The following resources are used for specific Module functions:

CHIP SELECTS LOGIC

CS0-0	FLASH ROM
CS1-0	STATIC RAM

SERIAL COMM CHANNELS

SCC1	PNET [RXD1, TXD1, RCLK1, TCLK1, CTS1-0, RTS1-0]
SCC2	ASYNC DEBUG [RXD2,TXD2]
SCP	SERIAL EEPROM [SPRXD,SPTXD,SPCLK]
TIMER1	SYSTEM TIMEBASE

PARALLEL IO / SPECIAL PURPOSE IO BITS

PA2	CHIP SELECT TO SERIAL EEPROM
PA5	ASYCN_EN (PNET MODE SELECT)
PA6	POWER MANAGEMENT CONTROL
PB5 /TIN2	TIMEBASE INPUT FOR EXTERNAL MEMORY / SYSTEM CONFIG
PB7	WATCHDOG TIMER OUTPUT

Program Memory

Program memory consists of two 8-bit flash ROMs U5 and U11 shown on sheet 5 of the schematic. The ROM is configured for 128Kx16 (2048k bit). The ROM is not socketed and can not be removed for programming. The ROM can be flash-programmed via the logic analyzer interface or the PNET connector.

Data Memory

Data is stored in two 8-bit static RAMs U3 and U12 shown on sheet 5 of the schematic. These RAMs are configured as 128Kx16. This RAM is cleared when power is removed.

Non-Volatile Memory

Serial EEPROM U1 shown on sheet 5 of the schematic is a 128-byte PROM that provides non-volatile storage for model and serial number information and parameter user interface data which must travel with the Module. The 68302 synchronous communication port (SCP) is used to access the EEPROM.

Logic Analyzer/Test Interface

The logic analyzer/test interface is shown on sheet 6 of the schematic. The core logic includes an interface to bring signals required for external ROM access, logic analyzer interface, and a debug serial channel to a single connector.

The external ROM access allows an off board ROM (8 bit) or ROMs (16 bit) to replace the FLASH devices at address 0. Address, data, and control signals required for this function are included on the LA/T connector.

All signals needed for a Hewlett Packard model 16500 logic analyzer or equivalent to perform bus state analysis and disassembly are included on the LA/T connector.

The 68302 SCC2 serial transmit and receive data signals are included on the LA/T connector.

The LA/T connector pinouts are as follows:

PIN	NAME	PIN	NAME
1,69	+5V	2,28,45,46,70	GND
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
29	D0	30	D1
31	D2	32	D3
33	D4	34	D5
35	D6	36	D7
37	D8	38	D9
39	D10	40	D11
41	D12	42	D13
43	D14	44	D15
47	DTACK-0	48	AS-0
49	RW	50	UDS-0
51	DS-0	52	BGACK-0
53	FC0	54	FC1
55	FC2	56	DEBUG TXD
57	DEBUGRXD	58	EXROMCS-0
63	PRGM_EN	64	DISCPU
65	T1_IN		

DISASSEMBLY PROCEDURE

STATIC DISCHARGE CAUTION

Do not attempt to service unit without static discharge protection. Workstations and personnel must be properly grounded, or damage to equipment will result.

1. Remove two 4-40 x 5-1/4" screws from rear of the Module. Remove rear cover.
2. Slide enclosure toward rear of Module, and remove enclosure.
3. Unsnap two tabs at top and two tabs at bottom of assembly, and remove insulators and card guides.
4. Remove the 4-40 x 1/4 screw (30, FO-8B) that fastens flex cable to the shield can.
5. Disconnect flex cable (14) from J101 on digital PWA (1).
6. Pull front panel away from assembled PWAs.
7. Carefully pull apart two PWA assemblies while disconnecting J100 on digital PWA.
8. Disassemble analog PWA shield assembly by disengaging each of the corner locking tabs (accessible through plastic shield vent openings).
9. Separate analog PWA from emi shield.
10. Using FO-8B as a guide, perform any additional disassembly that may be required for maintenance procedures.

REASSEMBLY PROCEDURE

1. Make sure the fastening tabs on emi shield cover (24, FO-8B) for analog PWA have not been deformed. Reassemble analog PWA and shield assembly.

2. Carefully join the two PWA assemblies while connecting J100 of digital PWA.

3. Slide front panel over assembled PWAs while connecting J3 of the front panel flex PWA (13).

4. Connect flex cable (14) to J101 of digital PWA.

5. Using 4-40 x 1/4 screw (30, FO-8B), secure flex terminal to ground shield on analog PWA. Tighten the screw to 4-in/lb.

6. Push upper and lower card guides onto slots of assembly.

7. Install insulators (13) so large notch end is toward rear of Module, to ensure integrity of patient safety isolation.

8. With enclosure oriented so large groove is at bottom and label is at right (viewed from front of Module), slide enclosure over front cover and assembly.

9. Install rear cover on the Module enclosure.

10. Fasten the front and rear covers to the enclosure by inserting two 4-40 x 5-1/4" screws from the rear through the enclosure to the front cover as shown in FO-8B. Tighten the two screws to 4-in/lb.

PARTS LISTS

ECG Module parts lists and location drawings are organized as follows:

Item	Parts List	Drawing
ECG Top Assembly	Table 8-1	FO-8B
ECG Digital PWA 315-546	Table 8-2	FO-8C
ECG Analog PWA 315-547	Table 8-3	FO-8D
ECG Analog PWA 315-548	Table 8-4	FO-8D
ECG Front Panel Flex PWA 313-108	Table 8-5	FO-8E
ECG Defib Sync Flex PWA 313-109	Table 8-1	FO-8F

Table 8-1. ECG Top Assembly Parts List

Item	Description	Part No.
1	PWA, ECG/RESP/TEMP DIGITAL	315-546
2	PWA, ECG3/RESP/TEMP, ANALOG	315-547
	PWA, ECG6/RESP/TEMP ANALOG	315-548
3	BRACKET, TEMPERATURE	704-923
4	BRACKET, DEFIB SYNC	704-924
6	SUB-ASSY, ENCLOSURE, EXTRUDED SW	320-676
7	COVER, PARAMETER REAR	703-188
8	PANEL, FRONT, ECG 3 LEAD	701-453
	PANEL, FRONT, ECG 6 LEAD	701-433
9	EMI SHIELD CAN, INTERNAL, ANALOG PWA	737-176
10	SCREW, RDH PHH, 4-40X51/8, CUSTOM	722-201
11	INSULATION, GUIDE, MODULE	750-182
13	PWA, FLEX, ECG6/FRONT PNL	313-108
14	PWA, FLEX, ECG DEFIB SYNC	313-109
J1	JACK, STEREO, 3.5 MM 3 CONDUCTOR	607-883
17	BUTTON, LATCH, SW	732-166
18	GASKET, ECG, FRONT PANEL	752-261
19	SPRING, CONTACT, GROUND	736-204
20	SCREW, 4-40X3/16 PNH PHH SST	719-101
21	SCREW, 4-40X1/4 PNH PHH SST	719-102
22	SCREW, 2-56X3/16 PNH PHH SST	719-237
23	DRESS NUT,TEMPERATURE	717-102
24	EMI SHIELD, EXTERNAL, ANALOG PWA	737-177
26	GASKET, DEFIB, FRONT PANEL	752-260
27	GASKET, TEMPERATURE, FRONT PANEL	752-259
28	INSULATOR, DIGITAL	750-189
29	EMI SHIELD, INTERNAL, DIGITAL PWA, ECG	737-184
30	SCREW, SELF TAPPING 4-24X1/4 PNH, PHH, SST	722-151
32	PAD, PORON, 1.5X0.5X0.125, ADHESIVE BACK	748-339

Table 8-2. ECG Digital PWA 315-546 Parts List

Item	Description	Part No.
C1,101,102, 104-108,128	CAP,2917/D,TANT,35V,20%,10 UF	606-188
C2,3	CAP,CER,SMD,0603,NPO,10%,50V,27 PF	605-718
C4-16,20-22, 114-125,129	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C109	CAP,2917/D,TANT,16V,20%,33 UF	606-111
C110	CAP,CER,SMD,0603,X7R,10%,50V,0.010 UF	605-821
C111	CAP,CER,SMD,1812,NPO,5%,50V,4700PF	603-702
C112	CAP,CER,SMD,1812,NPO,5%,50V,.010UF	603-701
C113	CAP,CER,SMD,1825,NPO,5%,50V,.018UF	603-700
C126	CAP,CER,SMD,0603,NPO,10%,50V,100 PF	605-725
CR1,13,100	DIODE, SCHOTTKY, 30V, 200MW, SOT-23	611-137
CR2-7,10,11, 104,105	DIODE, DUAL SERIES SMT SOT-23	611-140
CR12	DIO ZENER 6.2V, 5% SMT, 225MW	612-147
CR106,112	DIODE, RECT-SCHOTTKY, 1A, 40V, SMT	611-142
CR108-111	DIO SWI, 200 MA, 70V, SMD	610-114
FB1-9,100-102	FERRITE CHIP, EMI SUPPRESSION, SMT	669-170
J1	CONN, 20 PIN PLUG RT ANGLE PC MOUNT	607-795
J4	SOCKET, MICRO STRIP 35X2, SMD	607-816
J100	CONN, 20 PIN, RECEPT, .050 PITCH, SIP	608-348
J101	CONN, 5 POS, 1MM CTR, ZIF, SMT, RT ANGLE	607-921
L100	FILTER, DATA LINE (3-LINES)	668-162
PM1	PWR SUPPLY, DC TO DC 1.5W PC MT	633-147
Q1,90	XST NPN 2222A SMT	674-127
Q100-103	XSTR, N-CHAN MOS SOT-23	676-130
R1,40,41,50,112, 114,118,129, 131-133,150	RES,0603,1/16W,1%,1.00K OHM	686-293
R2,90	RES,0603,1/16W,1%,4.99K OHM	686-360
R3,4,7-33,35,42, 43,47,48,92,100, 111,115,117,130	RES,0603,1/16W,1%,10.0K OHM	686-389
R5,6,127,135, 136,140	RES,0603,1/16W,1%,2.21K OHM	686-326
R34	RES,0603,1/16W,1%,698K OHM	686-566
R45	RES,0603,1/16W,1%,100 OHM	686-197
R91,123,128	RES,0603,1/16W,1%,110K OHM	686-489

Table 8-2. ECG Digital PWA 315-546 Parts List (Continued)

Item	Description	Part No.
R109	RES,0603,1/16W,1%,49.9 OHM	686-168
R110,113,116,152	RES,0603,1/16W,1%,475 OHM	686-262
R119	RES,0603,1/16W,1%,22.1K OHM	686-422
R120,121	RES,0603,1/16W,1%,162K OHM	686-505
R122	RES,0603,1/16W,1%,44.2K OHM	686-451
R124	RES,0603,1/16W,1%,88.7K OHM	686-480
R125,126	RES,0603,1/16W,1%,20.5K OHM	686-419
R134	RES,0603,1/16W,1%,442K OHM	686-547
R138	RES,0603,1/16W,1%,49.9K OHM	686-456
R139,141	RES,0603,1/16W,1%,15.4 OHM	686-119
R142	RES,0603,1/16W,1%,11.3K OHM	686-394
R143	RES,0603,1/16W,1%,316K OHM	686-533
R144	RES,0603,1/16W,1%,57.6K OHM	686-462
R151	RES,0603,1/16W,JUMPER 0.0 OHM	686-606
U1	IC,93C56 2KBIT SERIAL EEPROM,CMOS SM	692-183
U2	IC, EECMOS PLD 16V8B, ARRAY LOGIC	692-226
U3,12	IC, 128X8 70NS CMOS SRAM TSOP	694-133
U4,15	IC,74AC32 QUAD 2 IN OR GATE,ADV CMOS SM	692-141
U5,11	IC, 128K X 8-BIT 5V FLASH ROM CMOS SMT	692-195
U6	IC,74HC03 QUAD 2 IN.NAND,CMOS SUF MT	692-139
U7,8	IC, CMOS LTC1485, DIFF BUS XCEIVER SO8	692-225
U9	IC, POWER SUPPLY MONT WITH RESET SMT	694-118
U10	IC, 68302 INTEGRATED PROCESSOR SUR MT	694-135
U100	IC, DUAL COMPARATOR SMD	693-158
U101-103	IC, HCPL-2611, OPTOCOUPLERS, SMT	695-101
U104	IC, 10 BIT DAC, SSOP	693-157
U105,106,111	IC, ADJ VOLTAGE REGULATOR SMT	693-119
U107,108	IC, 664 VOLTAGE REGULATOR SUR. MT.	693-104
U110	IC, DUAL JFET OP AMP SOIC	691-110
Y100	CRYSTAL, 23.646MHZ HC-49/UP	609-135
#73	PAL_U2A, CORE LOGIC	637-101

Table 8-3. ECG Analog PWA 315-547 Parts List

Item	Description	Part No.
C100,108,109, 116,117,119,198, 246,260	CAP,2312/C,TANT,16V,20%,10 UF	606-108
C101,102, 104-107,111, 113-115,118, 120,121,124,126, 127,130-134, 136,140,142,143, 145,146,148,150, 152-156, 160, 162-164,170,171, 175-178,181,183, 185,187,190,191, 193, 195,196, 199,203,207,213, 214,216-220,224, 233,237,238,240, 242-245,247-253, 255,256	CAP,CER,SMD,0603,Z5U,20%,50V,0.033 UF	605-919
C103	CAP,CER,SMD,0603,NPO,10%,50V,100 PF	605-725
C110,128,129, 137,192	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C112	CAP,2917/D,TANT,16V,20%,33 UF	606-111
C122,125,135, 138,159,209,211, 225	CAP,POLY,SMD,40VDC,10%,1.0UF	603-220
C123	CAP,CER,SMD,0603,X7R,10%,50V,0.010 UF	605-821
C139,254	CAP,CER,SMD,0805,X7R,10%,50V,4700 PF	605-517
C141	CAP,CER,SMD,0603,NPO,10%,50V,10 PF	605-713
C144,149,157, 161,167,169,182, 184,197,205,210, 223,228,230-232, 236,239	CAP,CER,SMD,1812,NPO,5%,50V,.010UF	603-701
C147,168,186, 204,208	CAP,0805,CER,NPO,5%,50V,330PF	603-630
C151,158,166, 202,206,212,215, 226,227,229,234, 235	CAP,0805,CER,NPO,5%,50V,1000PF	603-636

Table 8-3. ECG Analog PWA 315-547 Parts List (Continued)

Item	Description	Part No.
C165,188,189, 194	CAP,CER,SMD,0805,X7R,10%,50V,0.022 UF	605-525
C172,261-263	CAP,CER,SMD,0603,NPO,10%,50V,33 PF	605-719
C173,201,221, 222,257-259	CAP,0805,CER,NPO,5%,50V,100PF	603-624
C174	CAP,CER,SMD,0603,NPO,1%,50V,100PF	605-735
C179,180,200	CAP,POLYCARBONTE,3300PF,250V,5MM,5%	603-217
C241	CAP,CER,SMD,0805,Z5U,20%,50V,0.047 UF	605-621
CR100,121	DIO, SCHOTTKY, DUAL SERIES SOT-23 SMT	611-141
CR101,102, 105-107,109-111, 117-119,128	DIO SWI, 200 MA, 70V, SMD	610-114
CR103,104,108, 112,113	DIODE, DUAL SERIES SMT SOT-23	611-140
CR114-116, 125-127	DIODE, LOW LKG, DUAL SMT MMBD1503A	610-140
CR120,123	DIO, ZENER,2.5V,5%,225MW SMT	612-148
CR122,124	DIO, ZENER,5.1V,5%,225MW SURFACE MT	612-145
J100	CONN, 20 PIN, .050 PITCH, SIP HDR	608-349
J101	CONN, 10 POSN, DUAL ROW, RT ANGLE, 2MM	608-301
K100	RELAY, DIP, DPDT, 12V	648-113
Q100	XST PNP SMT	674-126
Q101,104	XSTR, N-CHAN MOS SOT-23	676-130
Q102,103,109, 110,111	XSTR, J-FET P-CHANNEL, SMD	676-134
Q105-108	XST NPN 2222A SMT	674-127
R100,102,103, 106,107,124-130, 132-134,136-142, 155-158,160-166, 169,173,223,226, 227,291,311,317, 327,341,343	RES,0603,1/16W,1%,100K OHM	686-485
R101,104,105, 113,117,119,144, 149,174,177,186, 187, 257,305, 306,308,339,342	RES,0603,1/16W,1%,10.0K OHM	686-389
R108,111	RES,0603,1/16W,1%,49.9 OHM	686-168
R109,171,258, 279,287,300	RES,0603,1/16W,1%,100 OHM	686-197

Table 8-3. ECG Analog PWA 315-547 Parts List (Continued)

Item	Description	Part No.
R110,131,172, 193,196,228,268, 347-349	RES,0603,1/16W,1%,1.00K OHM	686-293
R112	RES,0603,1/16W,1%,200 OHM	686-226
R114,115	RES,0603,1/16W,1%,3.01K OHM	686-339
R116	RES,0603,1/16W,1%,2.00K OHM	686-322
R118,123,152, 231,234,235	RES,0603,1/16W,1%,16.2K OHM	686-409
R120-122	RES,0603,1/16W,1%,30.9K OHM	686-436
R128,288,324, 332	RES,0603,1/16W,1%,280K OHM	686-528
R135,159,185, 191,297,323,326	RES,0603,1/16W,1%,49.9K OHM	686-456
R143	RES,0603,1/16W,1%,4.32K OHM	686-354
R145,146,192	RES,0603,1/16W,1%,24.3K OHM	686-426
R147,150,198, 199,202,203,207, 209,219,239,240, 247,248,260, 334,335	RES,0603,1/16W,1%,110K OHM	686-489
R148	RES,0603,1/16W,1%,44.2K OHM	686-451
R151,178,184	RES,SMD,1/10W,5%,10M OHM	685-605
R153	RES,MF,1.35K,0.05%,20 PPM/DEG C	652-342
R154	RES,MF,1.10K,0.01%, 10 PPM/DEG C	652-341
R168,170,244, 245,254,256, 277,280	RES,0603,1/16W,1%,20.5K OHM	686-419
R175,183,230, 364-367	RES,0603,1/16W,1%,20.0K OHM	686-418
R176,275,286, 289	RESISTOR, SMD, 1/8 WATT, 5%, 3.0M OHM	654-592
R179,255,276, 284	RES,0603,1/16W,1%,6.65K OHM	686-372
R180	RES,0603,1/16W,1%,4.64K OHM	686-357
R181,321,328, 337	RES,0603,1/16W,1%,61.9K OHM	686-465
R182,320,330, 338	RES,0603,1/16W,1%,41.2K OHM	686-448
R188,189,307	RES,0603,1/16W,1%,150K OHM	686-502
R190	RES,SMD,1/10W,5%,1.6M OHM	685-586
R194,221	RES,0603,1/16W,1%,19.1K OHM	686-416

Table 8-3. ECG Analog PWA 315-547 Parts List (Continued)

Item	Description	Part No.
R195,197,200, 232	RES,0603,1/16W,1%,4.75K OHM	686-358
R201	RES,0603,1/16W,1%,18.2K OHM	686-414
R204	RES,0603,1/16W,1%,7.50K OHM	686-377
R205,206,208, 212,216,220, 238,246,345,369	RES,0603,1/16W,1%,4.99K OHM	686-360
R210,252,274, 285	RES,0603,1/16W,1%,69.8K OHM	686-470
R211,241,253, 282	RES,0603,1/16W,1%,118K OHM	686-492
R213,215,242, 243,250,251,278, 281	RES,0603,1/16W,1%,48.7K OHM	686-455
R214,236,249, 273,283,309	RES,0603,1/16W,1%,52.3K OHM	686-458
R217,295,296, 298,322,325,331	RES,0603,1/16W,1%,12.4K OHM	686-398
R222,356	RES,0603,1/16W,1%,17.8K OHM	686-413
R224,225,290, 318,319,329, 333,336	RES,0603,1/16W,1%,25.5K OHM	686-428
R229	RES,0603,1/16W,1%,7.87K OHM	686-379
R233	RES,0603,1/16W,1%,143K OHM	686-500
R237,270,271	RESISTOR, SMD, 1/8 WATT, 1%, 499 OHM	654-264
R259,261-263	RES,0603,1/16W,1%,1.43K OHM	686-308
R264,292, 350-355,357-363	RES,0603,1/16W,1%,301K OHM	686-531
R265	RES,0603,1/16W,1%,2.67K OHM	686-334
R266,267	RES,0603,1/16W,1%,750 OHM	686-281
R269,293,294, 299,301-304	RES,0603,1/16W,1%,200K OHM	686-514
R272	RES,0603,1/16W,JUMPER 0.0 OHM	686-606
R310,312,313, 368,370,371	RES,SMD,1/4W,20%,100M WRAP TERM	687-100 or 687-108
R314-316, 372-374	RESISTOR, SMD, 1/8 WATT, 1%, 332K OHM	654-535
R340	RES,0603,1/16W,1%,499 OHM	686-264
R346	RES,0603,1/16W,1%,158K OHM	686-504
T100	XFORMER, ISOLATION, 1500V, DIP8	668-158

Table 8-3. ECG Analog PWA 315-547 Parts List (Continued)

Item	Description	Part No.
U100	IC, OP AMP MAX412, SMT	691-135
U101	IC, AD7872 14 BIT ADC, CMOS SMT	692-200
U102,126,127	IC, ANALOG MUX, CMOS SO-16	693-126
U103	IC, CMOS PROGRAM LOGIC DEVICE SMT	692-236
U104	IC, HEX SCHMITT-TRIGGER INVERTER, SMT	692-237
U105	IC, EPC1064 SERIAL EPROM 65K BIT	619-264
U106,132,137	IC,ANALOG MUX, 8 CHANNEL, SMT LOWLKG	691-125
U107,131	IC, DUAL JFET OP AMP, S0-8	691-116
U108	IC, DUAL COMPARATOR SMD	693-158
U109,111,113, 118,122,123,129, 130,136,138	IC, QUAD OP AMP SUR. MT.	691-119
U110,112, 116,117	IC, LIN, 8TH ORDER BESSEL FILTER, DIP8	621-253
U114,135	IC, MAX333A QUAD SPDT CMOS AN. SW SMT	692-201
U115	IC, OP AMP JFET INPUT, QUAD, WIDE SMT	691-142
U119,126, 133,134	IC, INSTR AMP, 50-8	691-122
U120	IC, 5V REG/TEMP XDCR, SMD	693-121
U121	IC, DUAL MOS PHOTO RELAY, SMT	695-104
U124	IC, QUAD SPST ANALOG SWITCH SUR MT	693-112
U128	IC, ANALOG MUX, MONOLITHIC 4-CHAN SMT	692-240
#71	SOCKET,DIP LO-PROFILE 8 PIN	607-165
#142	FPGA, INVASIVE PRESSURE/ECG	637-116

Table 8-4. ECG Analog PWA 315-548 Parts List

Item	Description	Part No.
C100,108,109, 116,117,119, 198,246,260	CAP,2312/C,TANT,16V,20%,10 UF	606-108
C101,102, 104-107,111, 113-115,118,120, 121,124,126,127, 130-134,136,140, 142,143,145,146, 148,150,152-156, 160,162-164,170, 171,175-178,181, 183,185,187,190, 191,193,195,196, 199,203,207,213, 214,216-220,224, 233,237,238,240, 242-245,247-253, 255,256	CAP,CER,SMD,0603,Z5U,20%,50V,0.033 UF	605-919
C103	CAP,CER,SMD,0603,NPO,10%,50V,100 PF	605-725
C110,128,129, 137,192	CAP,CER,SMD,0805,X7R,10%,50V,0.10 UF	605-533
C122,125,135, 138,159,209,211, 225	CAP,POLY,SMD,40VDC,10%,1.0UF	603-220
C123	CAP,CER,SMD,0603,X7R,10%,50V,0.010 UF	605-821
C139,254	CAP,CER,SMD,0805,X7R,10%,50V,4700 PF	605-517
C141	CAP,CER,SMD,0603,NPO,10%,50V,10 PF	605-713
C144,149,157, 161,167,169,182, 184,197,205,210, 223,228,230,231, 232,236,239	CAP,CER,SMD,1812,NPO,5%,50V,.010UF	603-701
C147,168,186, 204,208	CAP,0805,CER,NPO,5%,50V,330PF	603-630
C151,158,166, 202,206,212,215, 226,227,229, 234,235	CAP,0805,CER,NPO,5%,50V,1000PF	603-636
C165,188, 189,194	CAP,CER,SMD,0805,X7R,10%,50V,0.022 UF	605-525

Table 8-4. ECG Analog PWA 315-548 Parts List (Continued)

Item	Description	Part No.
C172,261-263	CAP,CER,SMD,0603,NPO,10%,50V,33 PF	605-719
C173,201,221, 222,257-259	CAP,0805,CER,NPO,5%,50V,100PF	603-624
C174	CAP,CER,SMD,0603,NPO,1%,50V,100PF	605-735
C179,180,200	CAP,POLYCARBONTE,3300PF,250V,5MM,5%	603-217
C241	CAP,CER,SMD,0805,Z5U,20%,50V,0.047 UF	605-621
CR100,121	DIO, SCHOTTKY, DUAL SERIES SOT-23 SMT	611-141
CR101,102, 105-107,109-111, 117-119,128	DIO SWI, 200 MA, 70V, SMD	610-114
CR103,104,108, 112,113	DIODE, DUAL SERIES SMT SOT-23	611-140
CR114-116, 125-127	DIODE, LOW LKG, DUAL SMT MMBD1503A	610-140
CR120,123	DIO, ZENER,2.5V,5%,225MW SMT	612-148
CR122,124	DIO, ZENER,5.1V,5%,225MW SURF. MNT	612-145
J100	CONN, 20 PIN, .050 PITCH, SIP HDR	608-349
J101	CONN, 10 POSN, DUAL ROW, RT ANGLE, 2MM	608-301
K100	RELAY, DIP, DPDT, 12V	648-113
Q100	XST PNP SMT	674-126
Q101-104	XSTR, N-CHAN MOS SOT-23	676-130
Q102,103, 109-111	XSTR, J-FET P-CHANNEL, SMD	676-134
Q105-108	XST NPN 2222A SMT	674-127
R100,102,103, 106,107,124-130, 132-134,136-142 155-158,160-166, 169,173,223,226, 227,291,311,317, 327,341,343	RES,0603,1/16W,1%,100K OHM	686-485
R101,104,105, 113,117,119,144, 149,177,186, 187,257,305,306, 308,339,342	RES,0603,1/16W,1%,10.0K OHM	686-389
R108,111	RES,0603,1/16W,1%,49.9 OHM	686-168
R109,171,258, 279,287,300	RES,0603,1/16W,1%,100 OHM	686-197

Table 8-4. ECG Analog PWA 315-548 Parts List (Continued)

Item	Description	Part No.
R110,172,193, 196,228,268, 347-349	RES,0603,1/16W,1%,1.00K OHM	686-293
R112	RES,0603,1/16W,1%,200 OHM	686-226
R114,115	RES,0603,1/16W,1%,3.01K OHM	686-339
R116	RES,0603,1/16W,1%,2.00K OHM	686-322
R118,123,152, 231,234,235	RES,0603,1/16W,1%,16.2K OHM	686-409
R120-122	RES,0603,1/16W,1%,30.9K OHM	686-436
R135,159,185, 191,297,323,326	RES,0603,1/16W,1%,49.9K OHM	686-456
R143	RES,0603,1/16W,1%,4.32K OHM	686-354
R145,146,192	RES,0603,1/16W,1%,24.3K OHM	686-426
R147,150,198, 199,202,203,207, 209,219,239,240 247,248,260, 334,335	RES,0603,1/16W,1%,110K OHM	686-489
R148	RES,0603,1/16W,1%,44.2K OHM	686-451
R151,178,184	RES,SMD,1/10W,5%,10M OHM	685-605
R153	RES,MF,1.35K,0.05%,20 PPM/DEG C	652-342
R154	RES,MF,1.10K,0.01%, 10 PPM/DEG C	652-341
R168,170,244, 245,254,256, 277,280	RES,0603,1/16W,1%,20.5K OHM	686-419
R175,183,230, 364-367	RES,0603,1/16W,1%,20.0K OHM	686-418
R176,275, 286,289	RESISTOR, SMD, 1/8 WATT, 5%, 3.0M OHM	654-592
R179,255, 276,284	RES,0603,1/16W,1%,6.65K OHM	686-372
R180	RES,0603,1/16W,1%,4.64K OHM	686-357
R181,321, 328,337	RES,0603,1/16W,1%,61.9K OHM	686-465
R182,320, 330,338	RES,0603,1/16W,1%,41.2K OHM	686-448
R188,189,307	RES,0603,1/16W,1%,150K OHM	686-502
R190	RES,SMD,1/10W,5%,1.6M OHM	685-586
R194,221	RES,0603,1/16W,1%,19.1K OHM	686-416
R195,197,200, 232	RES,0603,1/16W,1%,4.75K OHM	686-358

Table 8-4. ECG Analog PWA 315-548 Parts List (Continued)

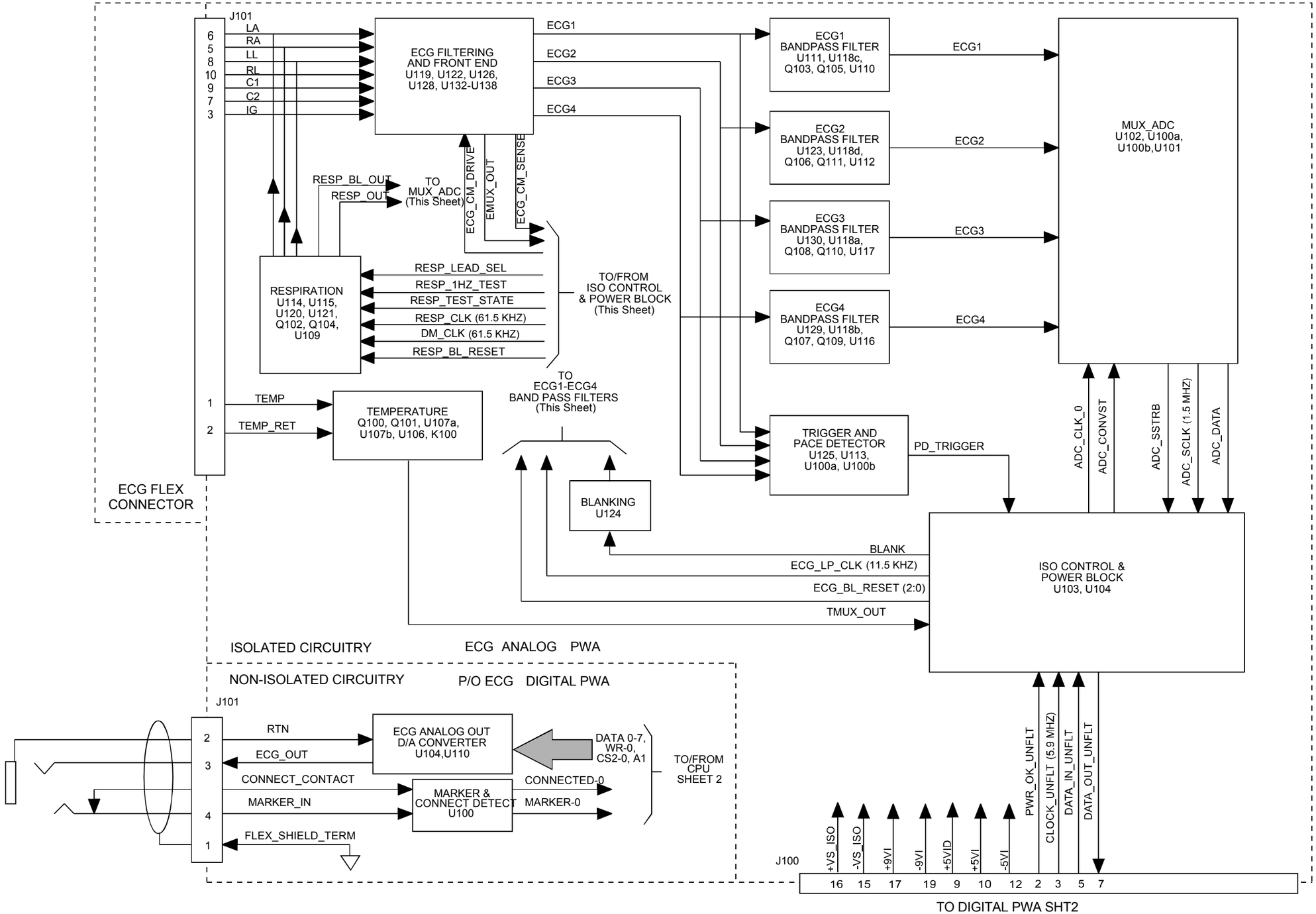
Item	Description	Part No.
R201	RES,0603,1/16W,1%,18.2K OHM	686-414
R204	RES,0603,1/16W,1%,7.50K OHM	686-377
R205,206,208, 212,216,220, 238,246,345,369	RES,0603,1/16W,1%,4.99K OHM	686-360
R210,252, 274,285	RES,0603,1/16W,1%,69.8K OHM	686-470
R211,241, 253,282	RES,0603,1/16W,1%,118K OHM	686-492
R213,215,242, 243,250,251, 278,281	RES,0603,1/16W,1%,48.7K OHM	686-455
R214,236,249, 273,283,309	RES,0603,1/16W,1%,52.3K OHM	686-458
R217,295,296, 298,322,325,331	RES,0603,1/16W,1%,12.4K OHM	686-398
R218,288, 324,332	RES,0603,1/16W,1%,280K OHM	686-528
R222,356	RES,0603,1/16W,1%,17.8K OHM	686-413
R224,225,290, 318,319,329, 333,336	RES,0603,1/16W,1%,25.5K OHM	686-428
R229	RES,0603,1/16W,1%,7.87K OHM	686-379
R233	RES,0603,1/16W,1%,143K OHM	686-500
R237,270,271	RESISTOR, SMD, 1/8 WATT, 1%, 499 OHM	654-264
R259,261-263	RES,0603,1/16W,1%,1.43K OHM	686-308
R264,292, 350-355,357-363	RES,0603,1/16W,1%,301K OHM	686-531
R265	RES,0603,1/16W,1%,2.67K OHM	686-334
R266,267	RES,0603,1/16W,1%,750 OHM	686-281
R269,293,294, 299,301-304	RES,0603,1/16W,1%,200K OHM	686-514
R272	RES,0603,1/16W,JUMPER 0.0 OHM	686-606
R310,312,313, 368,370,371,	RES,SMD,1/4W,20%,100M WRAP TERM.	687-100 or 687-108
R314-316, 372-374	RESISTOR, SMD, 1/8 WATT, 1%, 332K OHM	654-535
R340	RES,0603,1/16W,1%,499 OHM	686-264
R346	RES,0603,1/16W,1%,158K OHM	686-504

Table 8-4. ECG Analog PWA 315-548 Parts List (Continued)

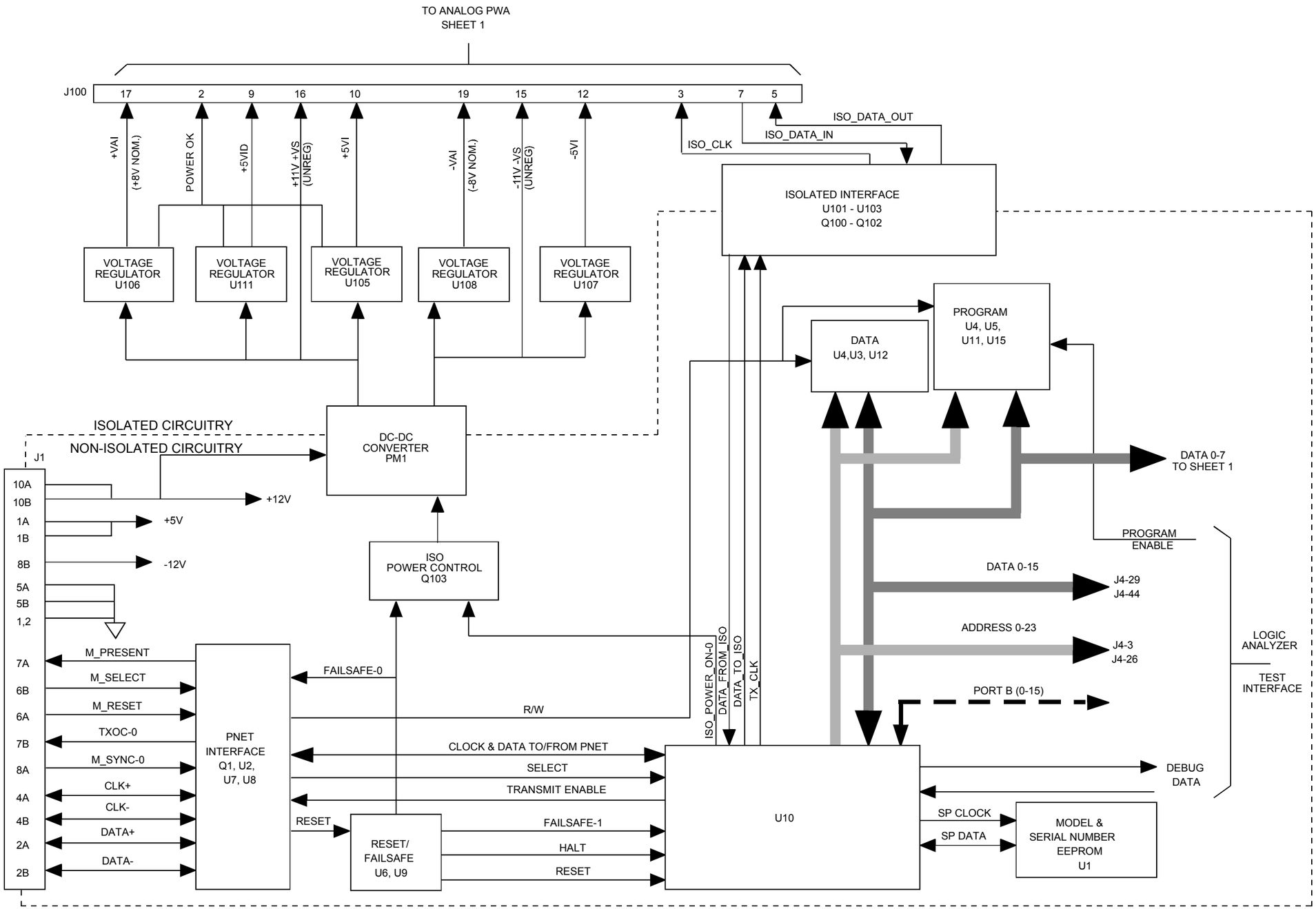
Item	Description	Part No.
T100	XFORMER, ISOLATION, 1500V, DIP8	668-158
U100	IC, OP AMP MAX412, SMT	691-135
U101	IC, AD7872 14 BIT ADC, CMOS SMT	692-200
U102,125,127	IC, ANALOG MUX, CMOS SO-16	693-126
U103	IC, CMOS PROGRAMM. LOGIC DEVICE SMT	692-236
U104	IC, HEX SCHMITT-TRIGGER INVERTER, SMT	692-237
U105	IC, EPC1064 SERIAL EPROM 65K BIT	619-264
U106,132,137	IC,ANALOG MUX, 8 CHANNEL, SMT LOWLKG	691-125
U107,131	IC, DUAL JFET OP AMP, S0-8	691-116
U108	IC, DUAL COMPARATOR SMD	693-158
U109,111,113, 118,122,123,129, 130,136,138	IC, QUAD OP AMP SUR. MT.	691-119
U110,112, 116,117	IC, LIN, 8TH ORDER BESSEL FILTER, DIP8	621-253
U114,135	IC, MAX333A QUAD SPDT CMOS AN. SW SMT	692-201
U115	IC, OP AMP JFET INPUT, QUAD, WIDE SMT	691-142
U119,126, 133,134	IC, INSTR AMP, 50-8	691-122
U120	IC, 5V REG/TEMP XDCR, SMD	693-121
U121	IC, DUAL MOS PHOTO RELAY, SMT	695-104
U124	IC, QUAD SPST ANALOG SWITCH SUR MT	693-112
U128	IC, ANALOG MUX, MONOLITHIC 4-CHAN SMT	692-240
#71	SOCKET,DIP LO-PROFILE 8 PIN	607-165
#142	FPGA, INVASIVE PRESSURE/ECG	637-116

Table 8-5. ECG Front Panel Flex PWA 313-108 Parts List

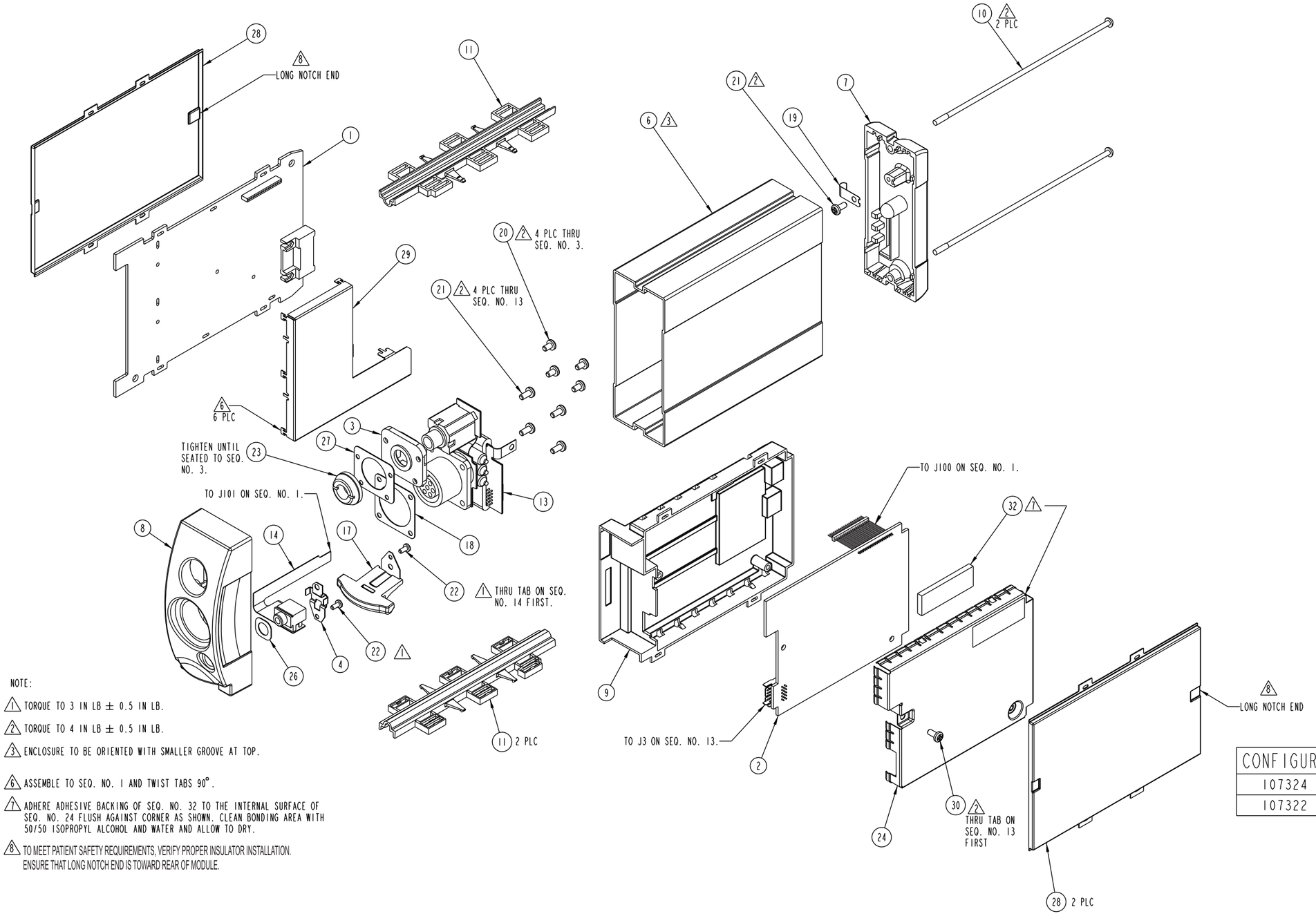
Item	Description	Part No.
C1-2	CAP,CER,SMD,0805,X7R,10%,50V,0.010 UF	605-521
C3-8	CAP,CER,SMD,0805,NPO,10%,200VDC,220PF	605-444
DS1-3	SURGE ARRESTER 2-LINE 80V GAS TUBE	628-165
J1	CONN, 7 PIN SOCKET ECG	607-887
J2	JACK, PHONE, 1/4 INCH 3 CONDUCTOR	607-884
J3	CONN, 10 POSN, DUAL ROW, 2MM	608-300
R1-6	RESISTOR, SMD, 1/8 WATT, 1%, 499 OHM	654-264
#3	CONTACT, SOCKET, POSTED FOR .025 SQ	608-266
#10	FERRITE CORE, FPC EMI SUPPRESSION	669-210



FO-8A. ECG Module Block Diagram (1 of 2)



FO-8A. ECG Module Block Diagram (2 of 2)



NOTE:

1. TORQUE TO 3 IN LB ± 0.5 IN LB.
2. TORQUE TO 4 IN LB ± 0.5 IN LB.
3. ENCLOSURE TO BE ORIENTED WITH SMALLER GROOVE AT TOP.
6. ASSEMBLE TO SEQ. NO. 1 AND TWIST TABS 90°.
7. ADHERE ADHESIVE BACKING OF SEQ. NO. 32 TO THE INTERNAL SURFACE OF SEQ. NO. 24 FLUSH AGAINST CORNER AS SHOWN. CLEAN BONDING AREA WITH 50/50 ISOPROPYL ALCOHOL AND WATER AND ALLOW TO DRY.
8. TO MEET PATIENT SAFETY REQUIREMENTS, VERIFY PROPER INSULATOR INSTALLATION. ENSURE THAT LONG NOTCH END IS TOWARD REAR OF MODULE.

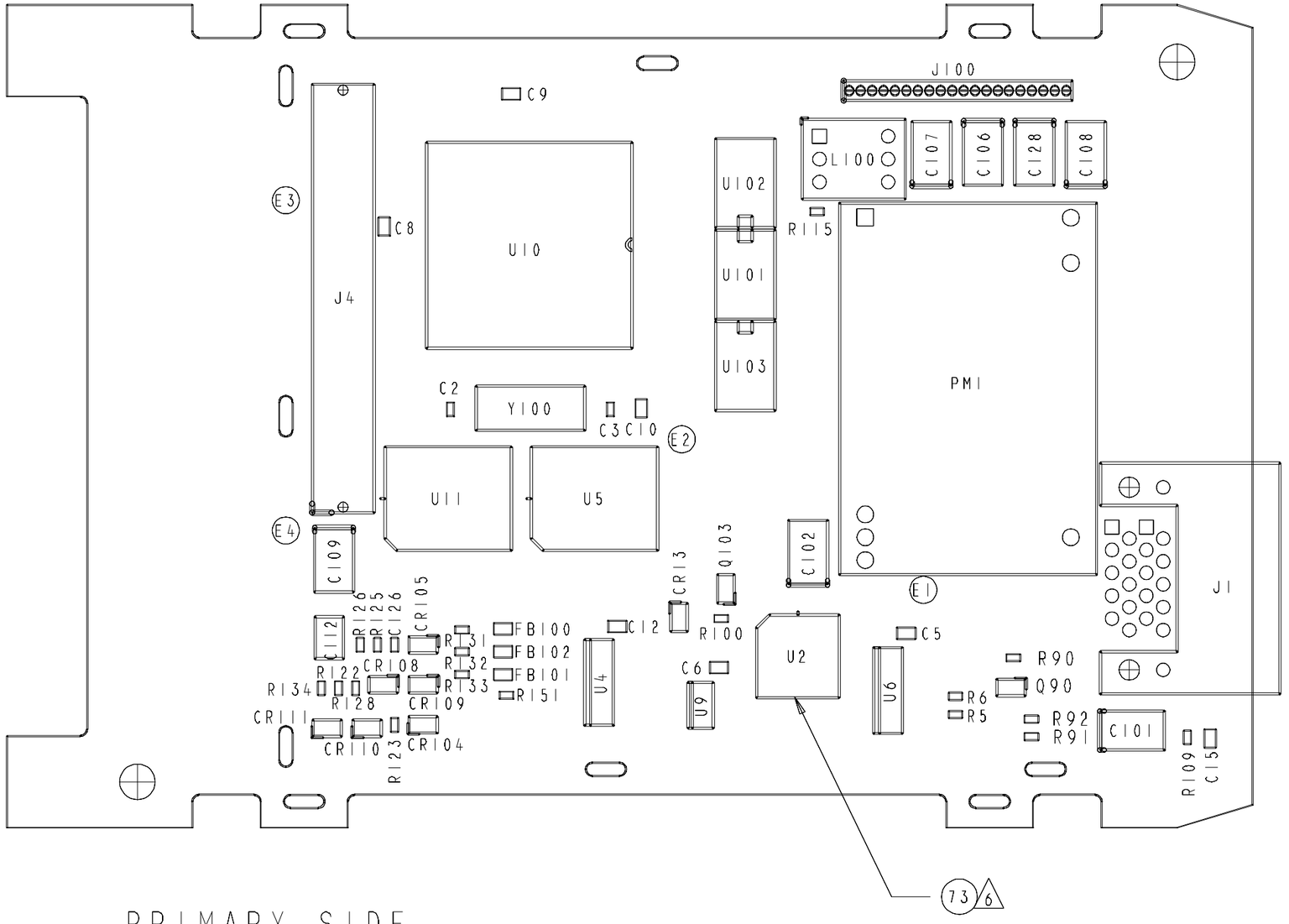
CONFIGURATION CHART	
107324	ECG VI
107322	ECG III

FO-8B. ECG Top Assembly

NOTES:

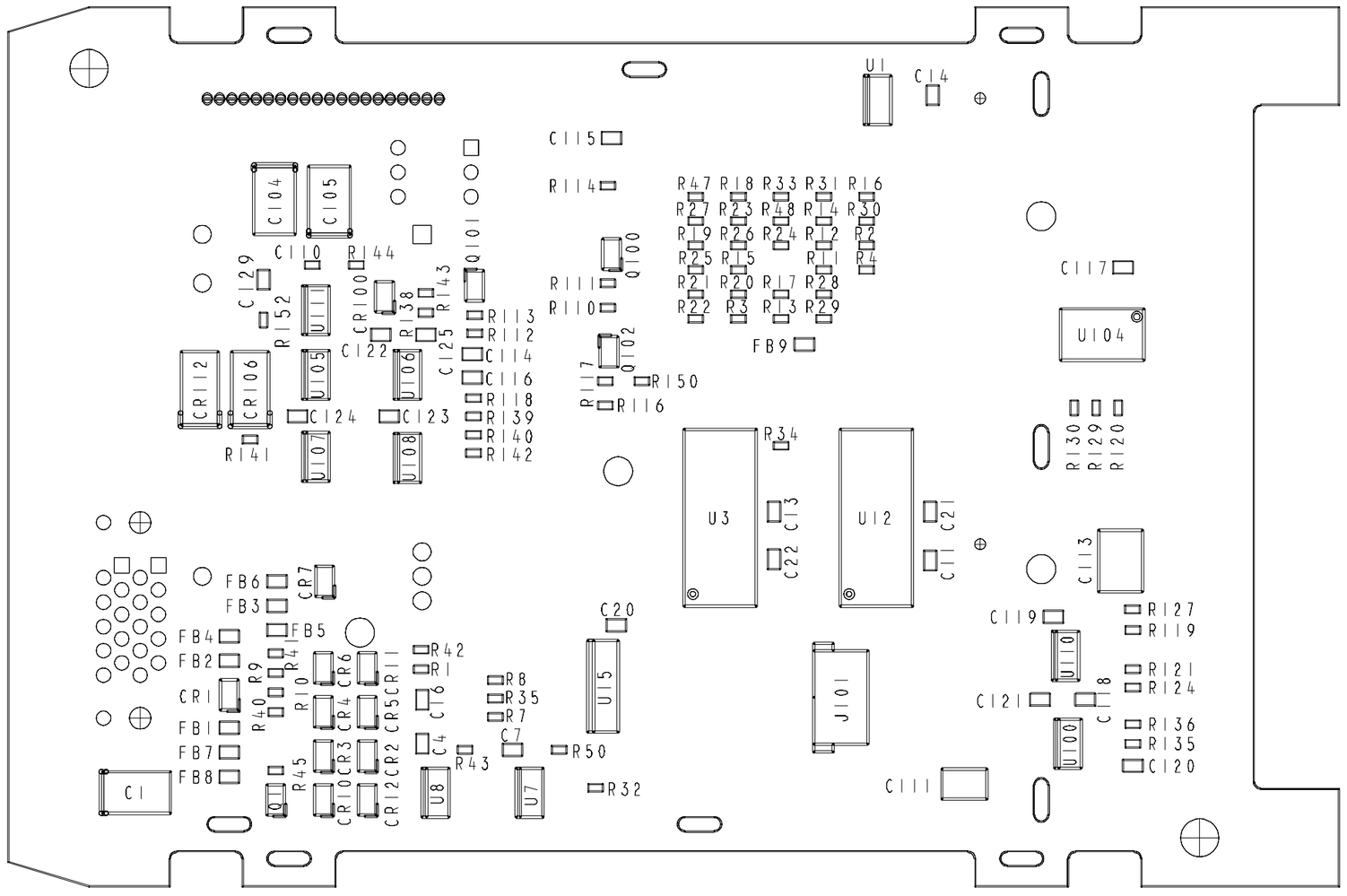
3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

△6 PROGRAM DEVICE PRIOR TO INSTALLATION.



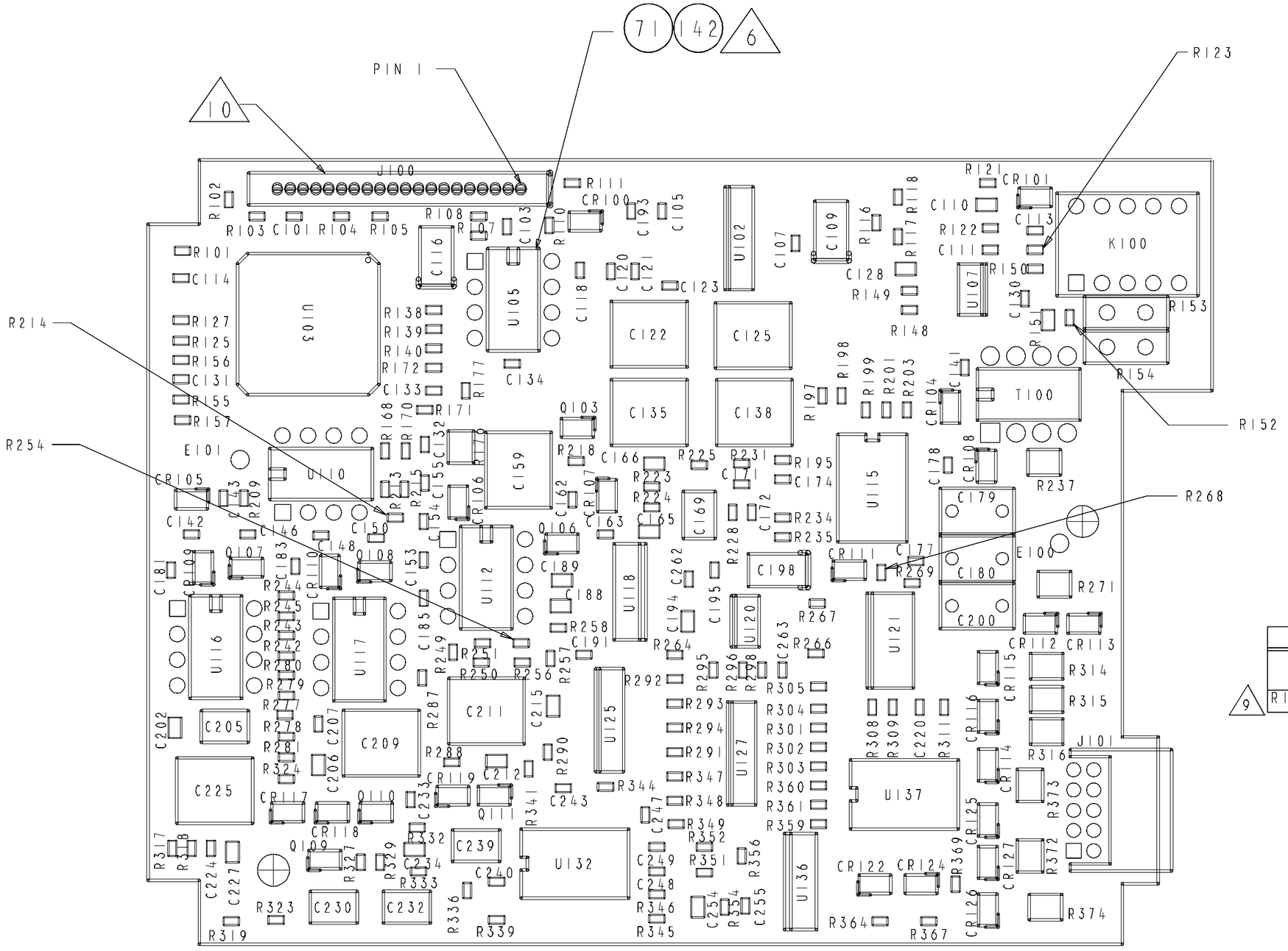
PRIMARY SIDE

FO-8C. ECG Digital PWA 315-546 (1 of 2)

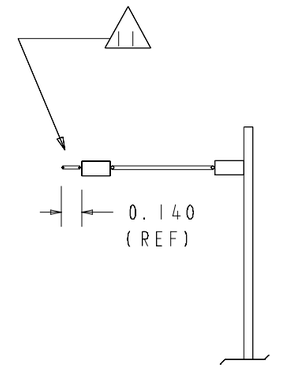


SECONDARY SIDE

FO-8C. ECG Digital PWA 315-546 (2 of 2)



COMPONENT PRIMARY



DETAIL A

CONFIGURATION TABLE		
	315548 6 LEAD ECG	315547 3 LEAD ECG
9 R131	DO NOT INSTALL	INSTALL

FO-8D. ECG Analog PWA 315-548 (1 of 2)

NOTES:

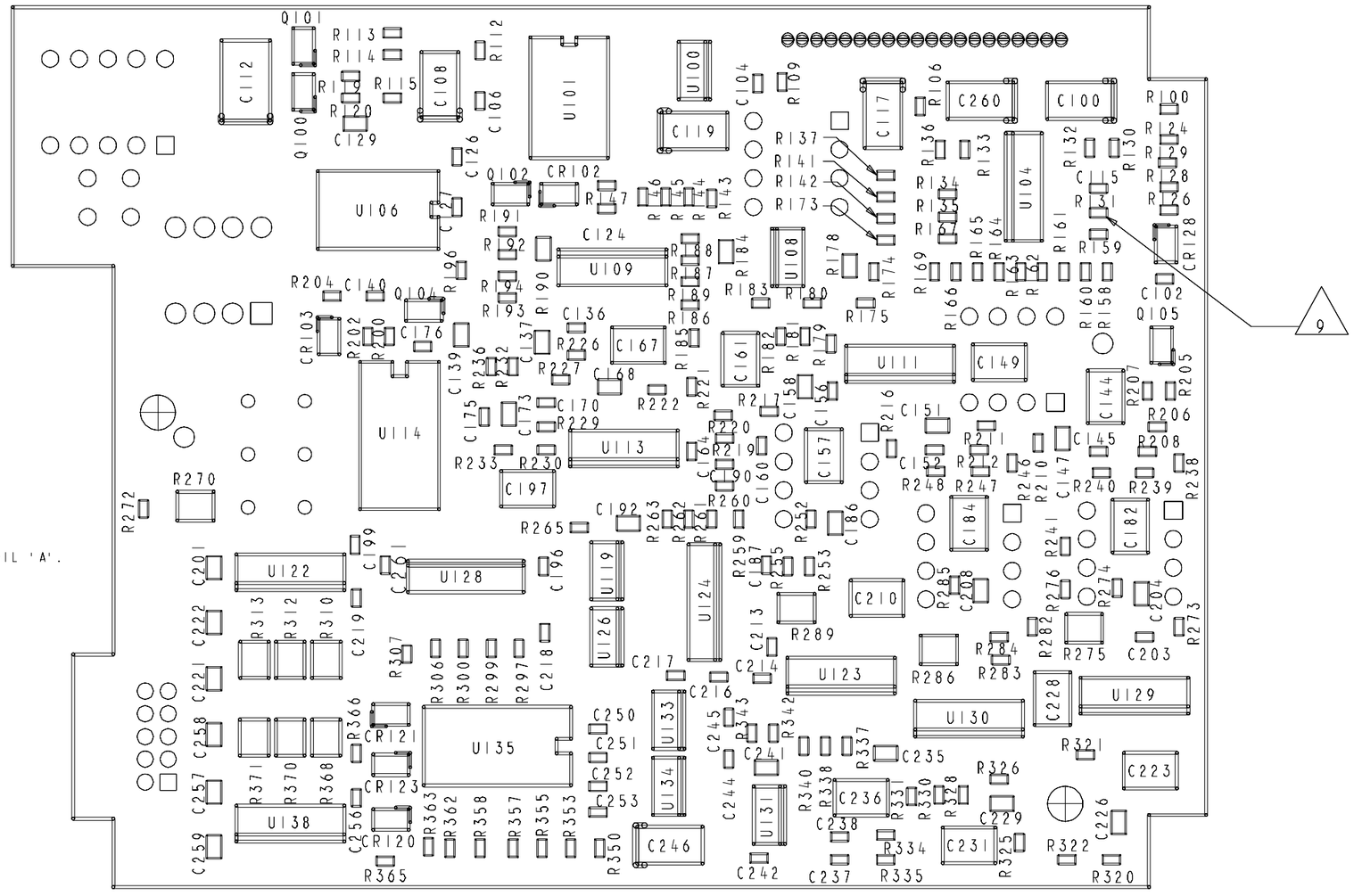
3. PIN NUMBER 1 IS INDICATED BY MARKINGS AND/OR SQUARE PAD.

6. PROGRAM (SEQ NO.142) DEVICE (SEQ NO.19) BEFORE INSTALLATION.

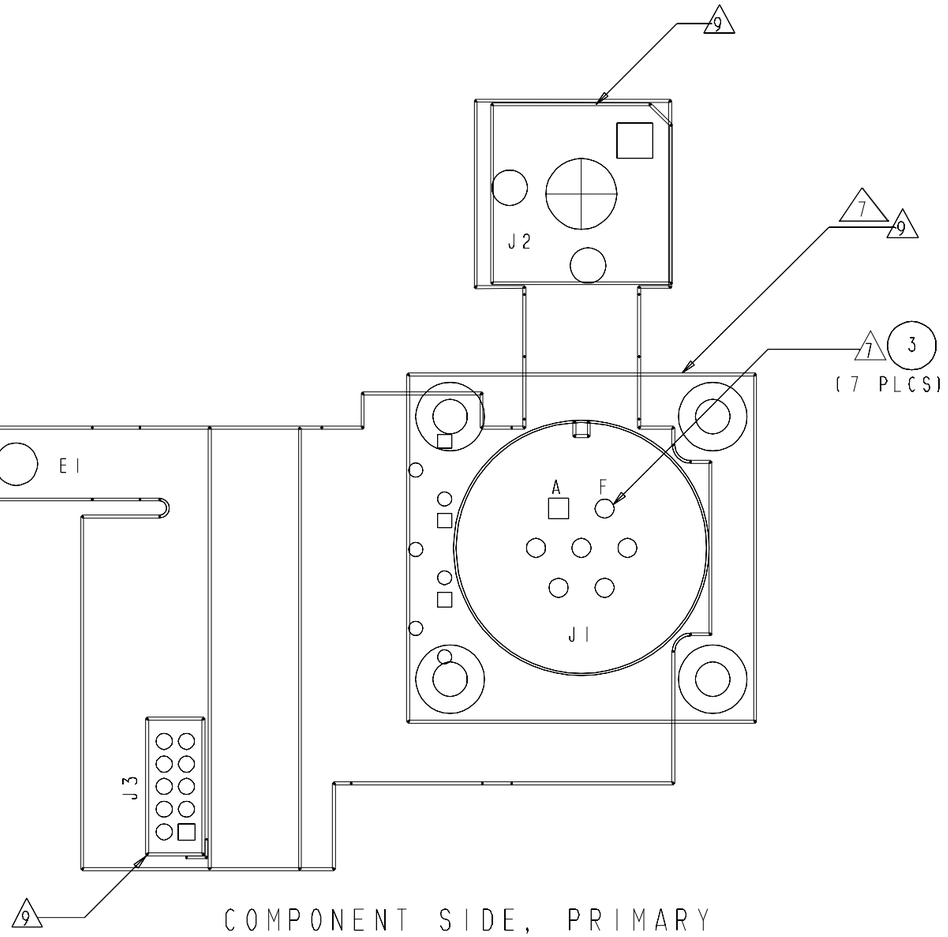
9. SEE CONFIGURATION TABLE.

10. MAX LEAD PROTRUSION 0.040" THROUGH PWB FOR J100.

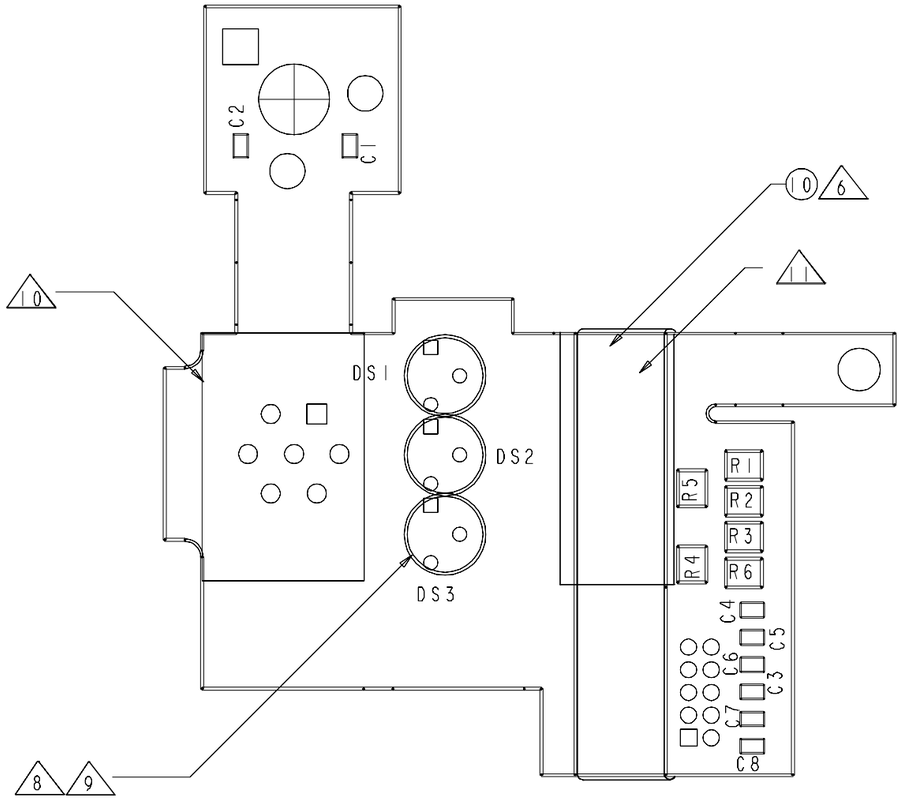
11. INSTALL J100 SO THAT THE LEAD PROTRUSION IS AS SHOWN IN DETAIL 'A'.

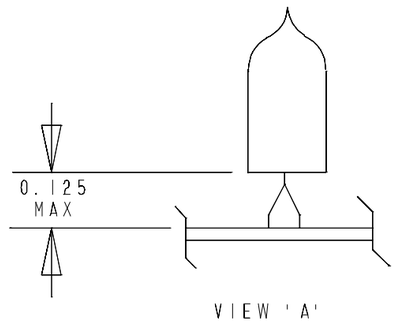


COMPONENT SECONDARY



COMPONENT SIDE, PRIMARY





VIEW 'A'

NOTES:

3 - PIN NUMBER 1 SHOWN AS SQUARE PAD FOR CONNECTORS.

6 - SLIDE FERRITE CORE(SEQ NO.10) ONTO CABLE AS BETWEEN SILKSCREEN LOCATORS AS SHOWN. SECURE FERRITE WITH 3M 2216 B/A GRAY EPOXY ADHESIVE OR EQUIVALENT.

7 - CRIMP BARREL OF SOCKET (SEQ NO.3) CONTACT TERMINAL WITH AMP TOOL 90277-1 OR EQUIVALENT TO APPROXIMATELY 0.125 DIAMETER, PRIOR TO PIN INSERTION INTO CONNECTOR J1. ENSURE CONTACT PINS LOCK IN CONNECTOR, PRIOR TO SOLDERING TO FLEX ASSEMBLY.

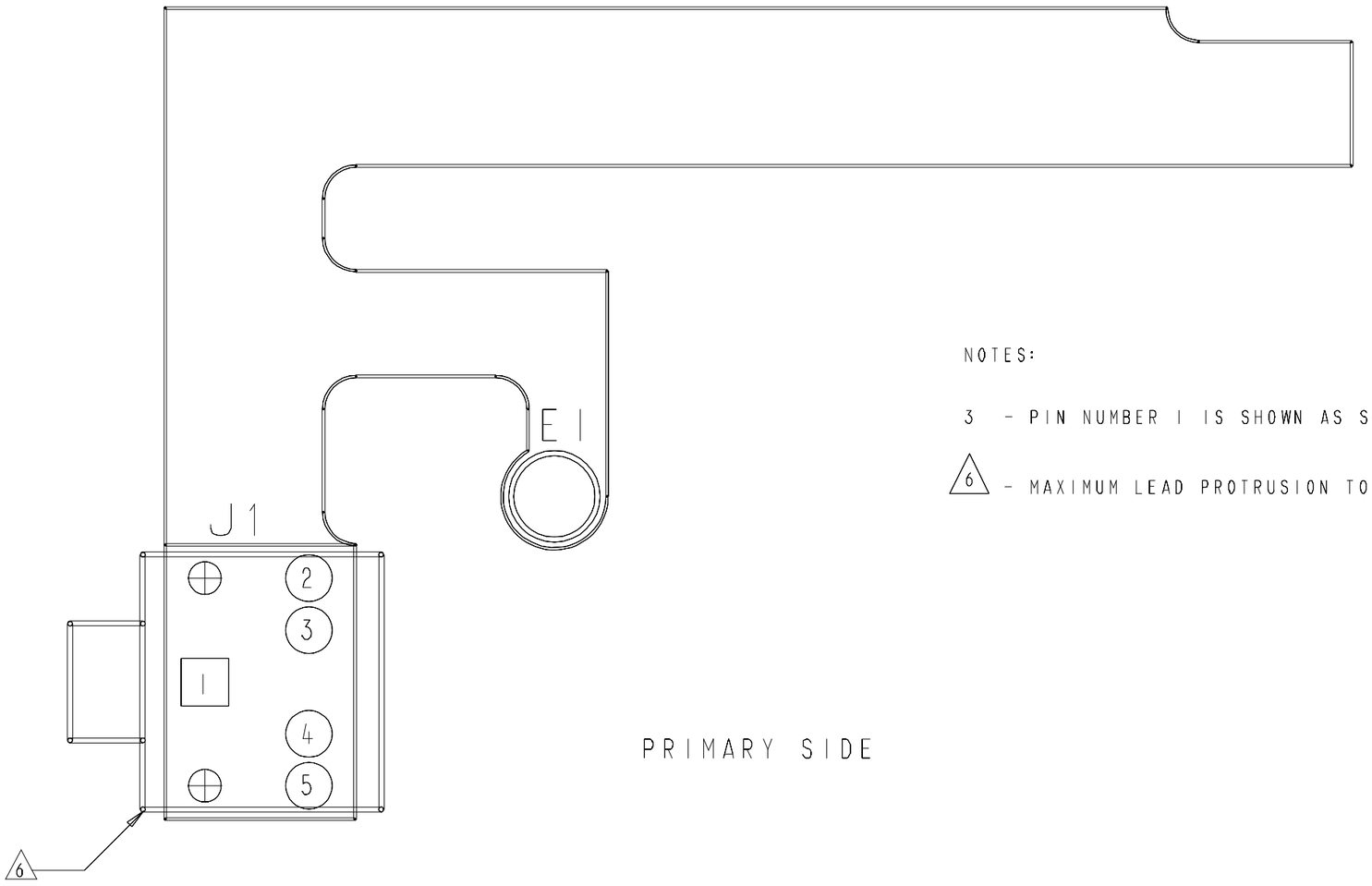
8 - MAXIMUM LEAD HEIGHT FOR SURGE PROTECTORS IS 0.125 MAX. SEE VIEW 'A'.

9 - MAXIMUM LEAD PROTRUSION AFTER SOLDERING TO BE LESS THAN 0.040.

10 - CUT FOAM TAPE APPROX. 1" X 0.5" AND PLACE ADHESIVE SIDE OVER APPROX. AREA AS SHOWN.

11 - CUT FOAM TAPE APPROX. 1" X 0.3" AND PLACE ADHESIVE SIDE OVER APPROX. AREA AS SHOWN.

FO-8E. ECG Front Panel Flex PWA 313-108

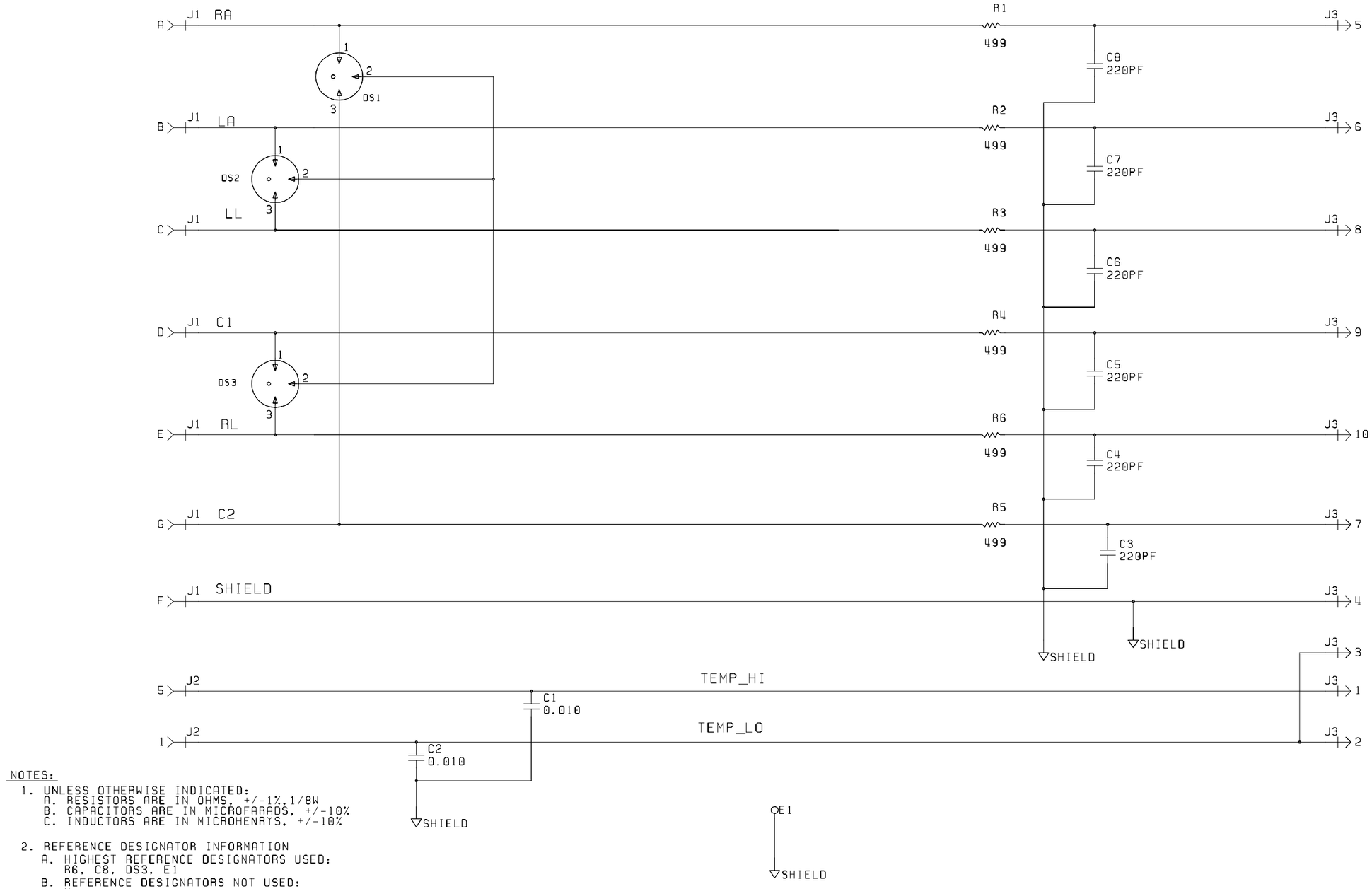


NOTES:

3 - PIN NUMBER 1 IS SHOWN AS SQUARE PAD FOR CONNECTORS.

6 - MAXIMUM LEAD PROTRUSION TO BE 0.040.

PRIMARY SIDE

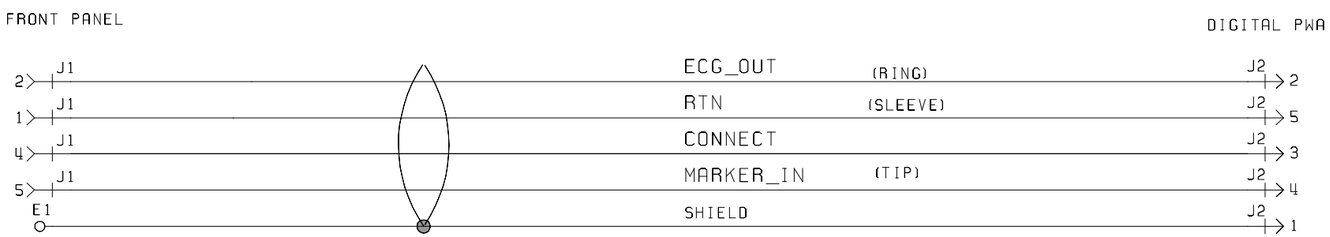


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/8W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      R6, C8, DS3, E1
   B. REFERENCE DESIGNATORS NOT USED:
      None

SC313-108 A
ECG Front Panel Flex PWA Schematic (1 of 1)



NOTES ON SHIELDING

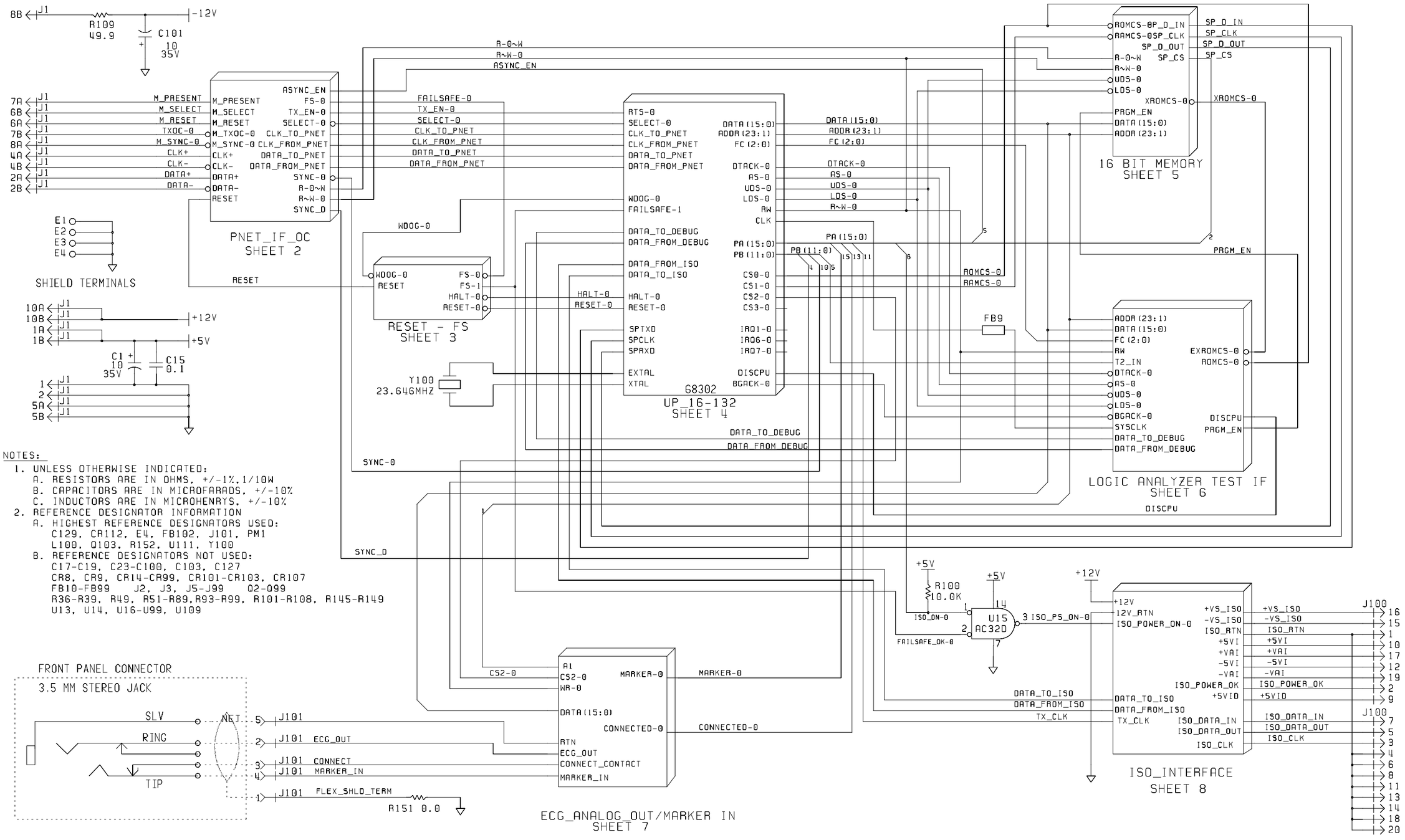
1. ALL SIGNALS TO BE ENCLOSED BY SHIELD LAYERS
2. E1 IS SHIELD TERMINATION TO FRONT PANEL METAL
3. J2 -1 IS SHIELD TERMINATION TO DIGITAL PWA

NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/8W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      J2, E1
   B. REFERENCE DESIGNATORS NOT USED:
      None

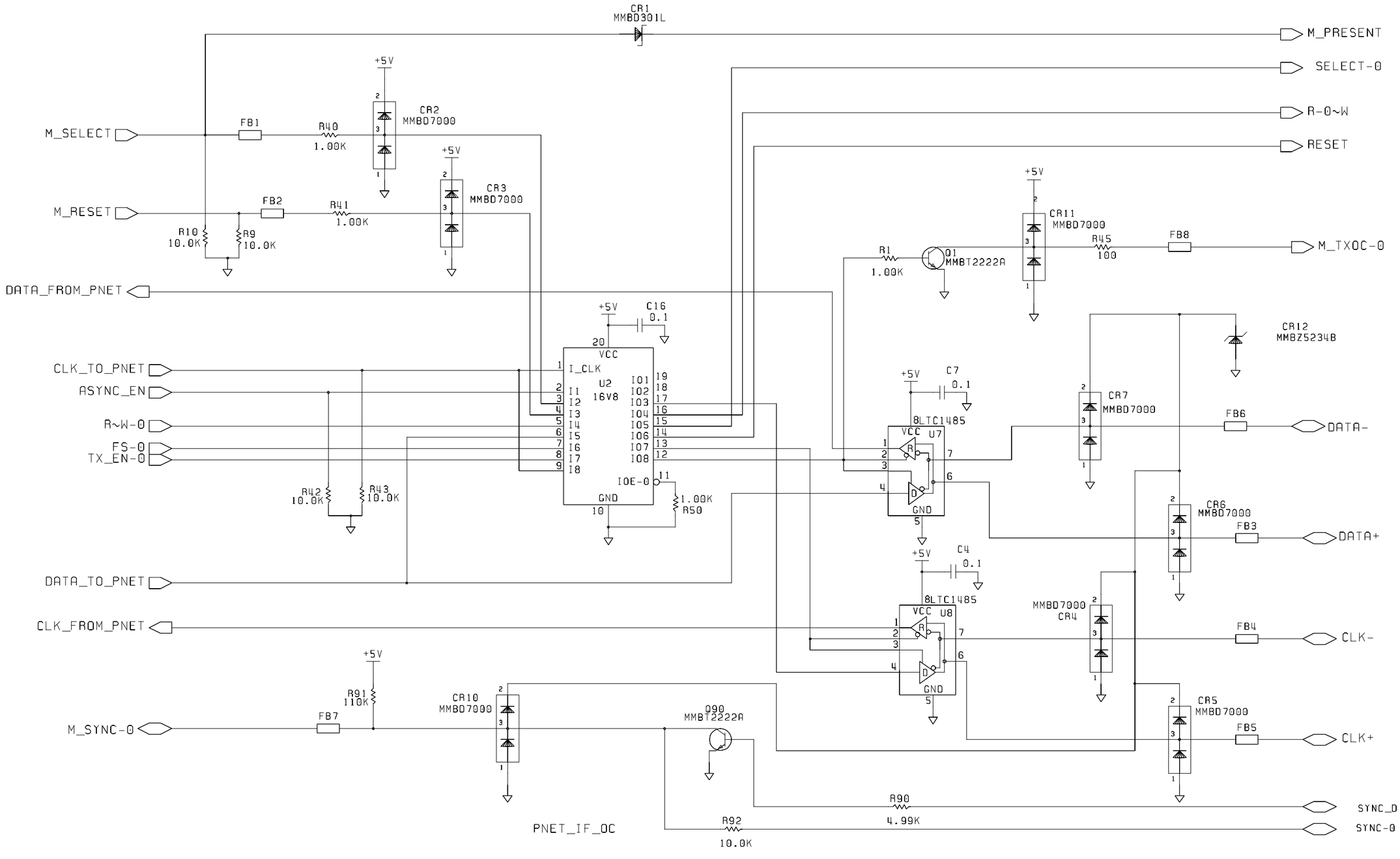
SC313-109 A
ECG Defib Sync Flex PWA Schematic (1 of 1)



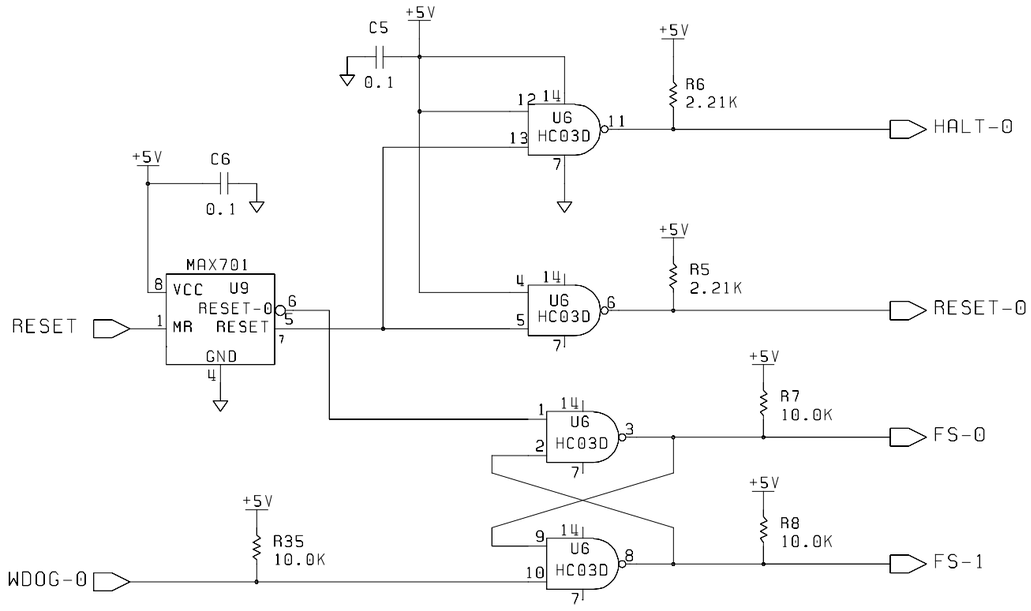
NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%,1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%
2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C129, CR112, E4, FB102, J101, PM1
      L100, Q103, R152, U111, Y100
   B. REFERENCE DESIGNATORS NOT USED:
      C17-C19, C23-C100, C103, C127
      CR8, CR9, CR14-CR99, CR101-CR103, CR107
      FB10-FB99 J2, J3, J5-J99 Q2-Q99
      R36-R39, R49, R51-R89,R93-R99, R101-R108, R145-R149
      U13, U14, U16-U99, U109

SC315-546 A
ECG Digital PWA Schematic (1 of 9)

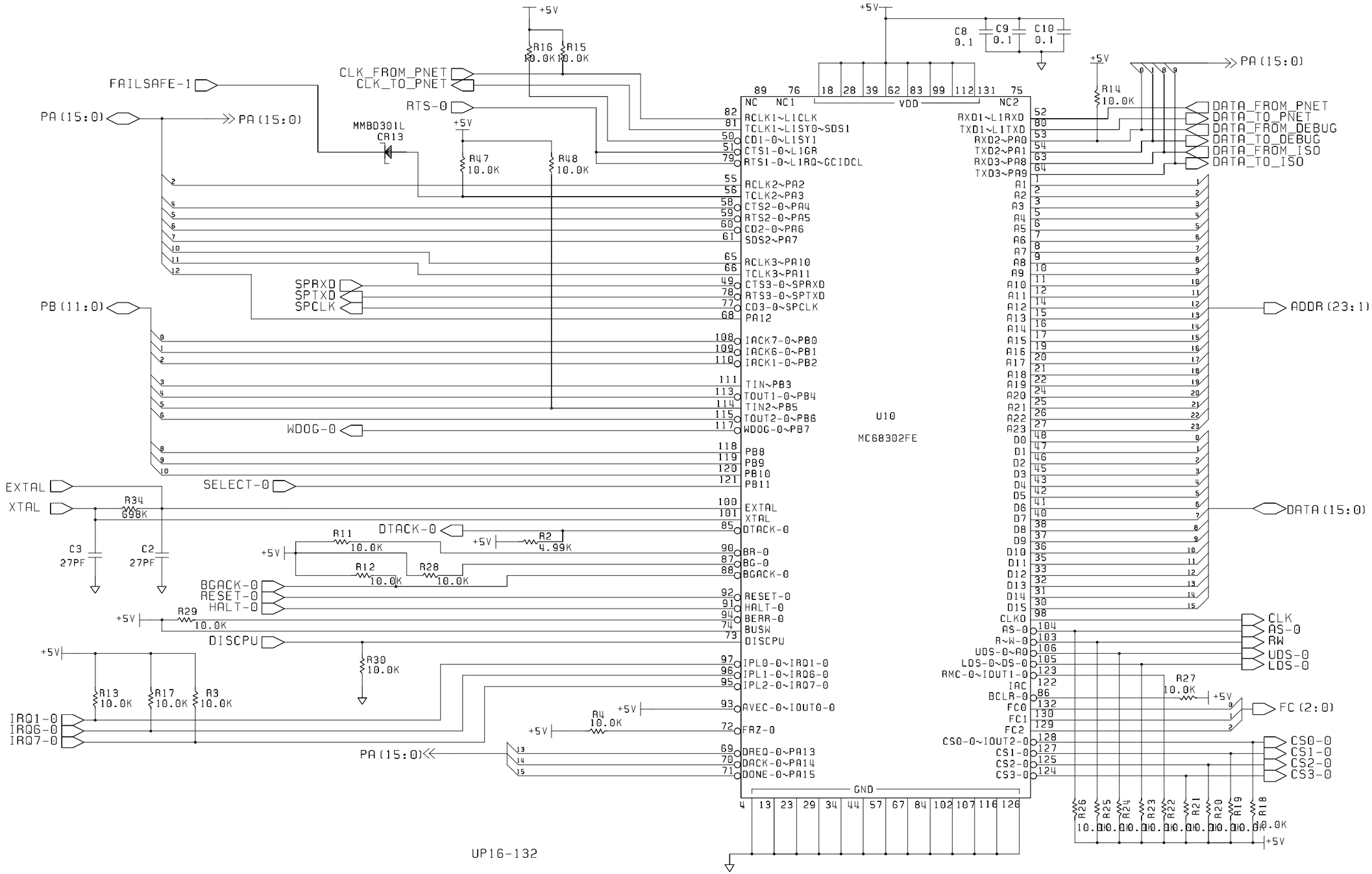


SC315-546 A
ECG Digital PWA Schematic (2 of 9)



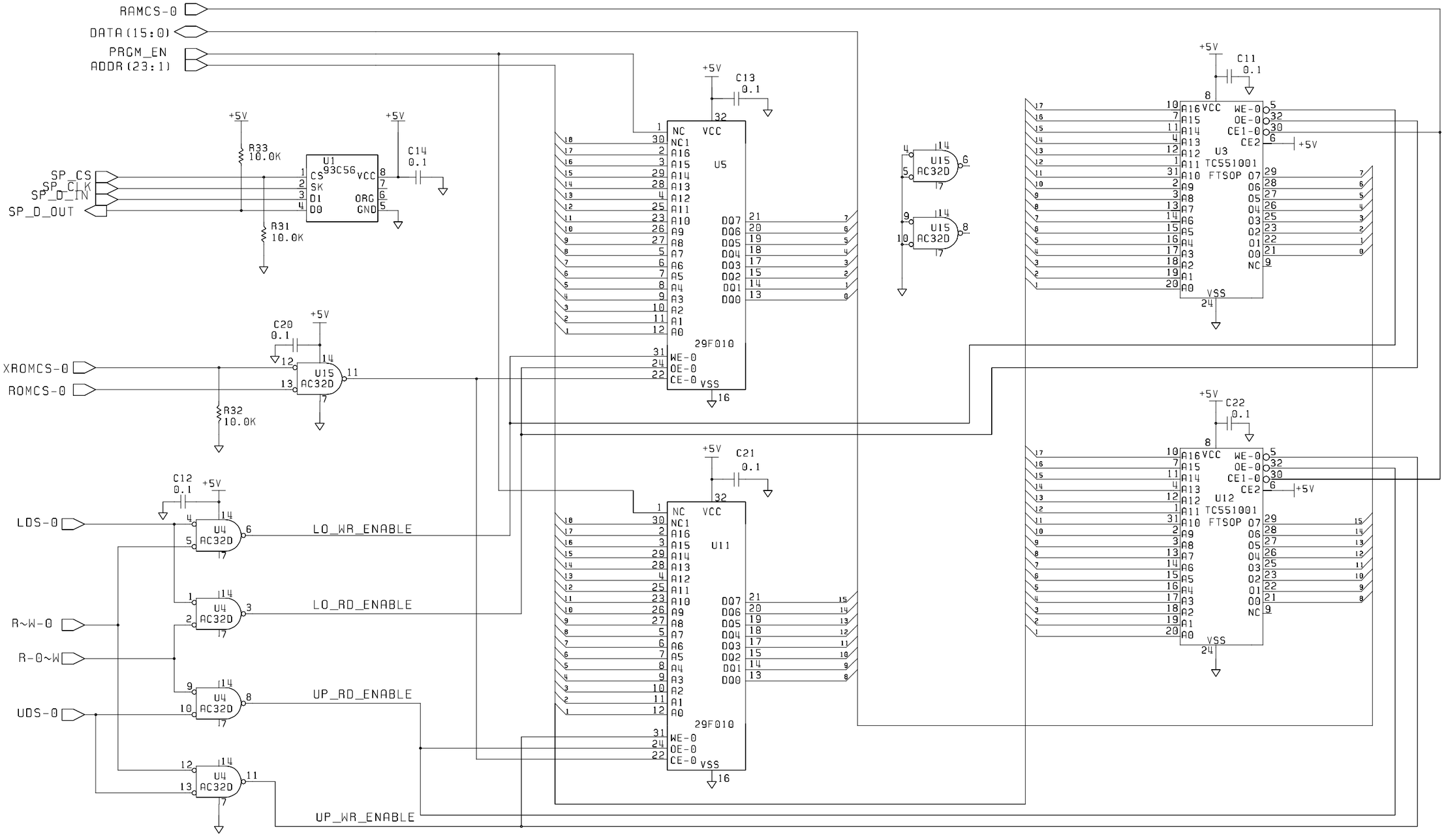
RESET - FS

SC315-546 A
ECG Digital PWA Schematic (3 of 9)



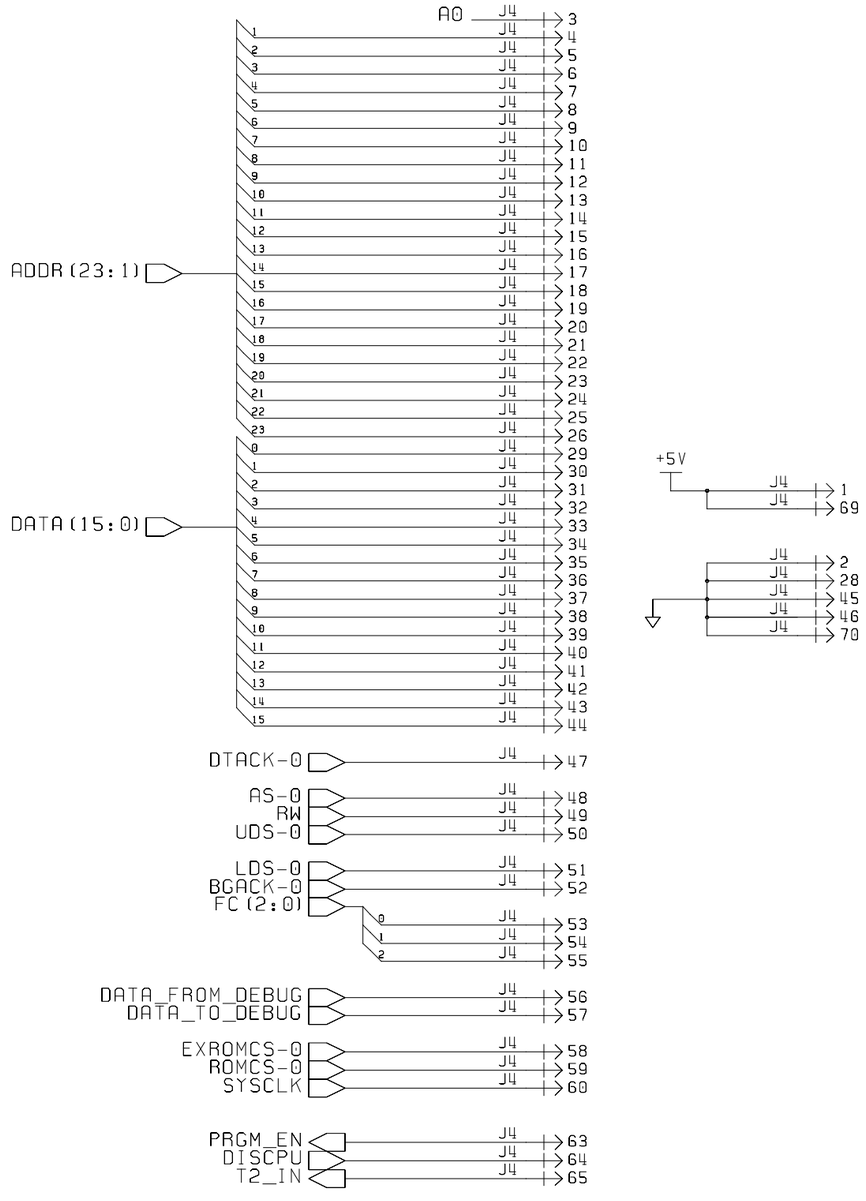
UP16-132

SC315-546 A
ECG Digital PWA Schematic (4 of 9)



16 BIT MEMORY

SC315-546 A
ECG Digital PWA Schematic (5 of 9)



LOGIC ANALYZER TEST IF

SC315-546 A
ECG Digital PWA Schematic (6 of 9)

DAC ADDRESS:
CS2+1=LOWER 8BITS (2 LSBS MUST BE 0)
CS2+3=HIGH NIBBLE
(odd byte addresses)
write lower byte first

A1
CS2-0
WR-0

DATA(15:0)

+5V
R130
10.0K
C117
0.1
U104
MAX503
CLR-0
A0
A1
CS-0
WR-0
LDAC-0
D6_S0
D7_S1
D8_D0
D9_D1
D2
D3
D4
D5
VDD
VOUT
RFB
ROFS
REFOUT
REFIN
VSS
REFGND
AGND
DGND
C109
33
R129
1.00K

R122
44.2K
R123
110K
C112
0.010
5%
R121
162K
C111
4700PF
5%
R120
162K
R124
88.7K
C113
0.018
5%
-12V
U110
TL082
R119
22.1K
C118
0.1
C119
0.1
+12V
-12V
CR104
MMBD7000
R133
1.00K
FB101
ECG_OUT
RTN

U100
LM393

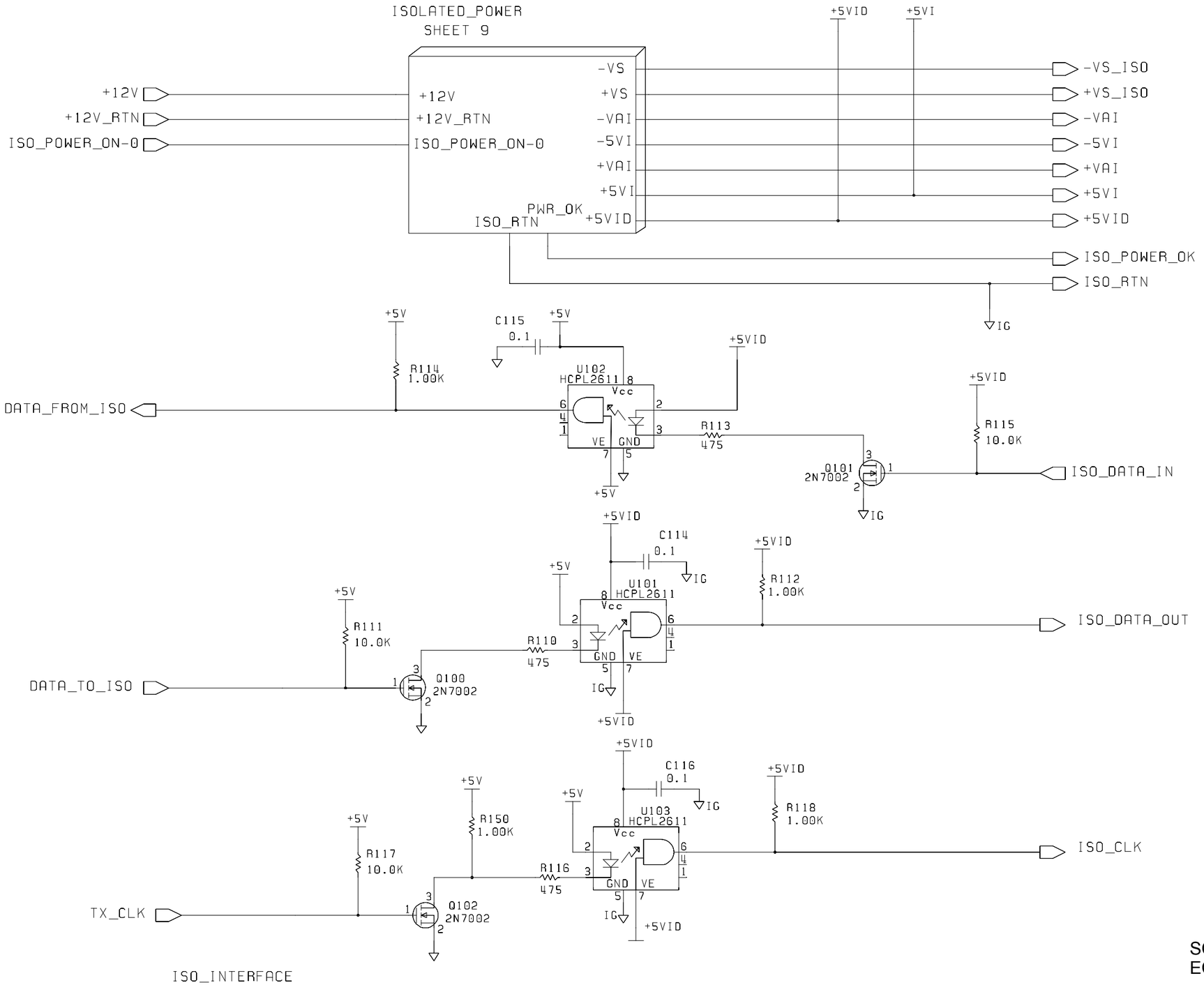
R134
442K
R125
20.5K
R126
20.5K
C121
0.1
C120
0.1
R136
2.21K
R135
2.21K
R127
2.21K
CR111
MMBD914X
CR110
MMBD914X

MARKER_IN
FB100
R131
1.00K
CR105
MMBD7000
C126
100PF
-12V
MARKER-0

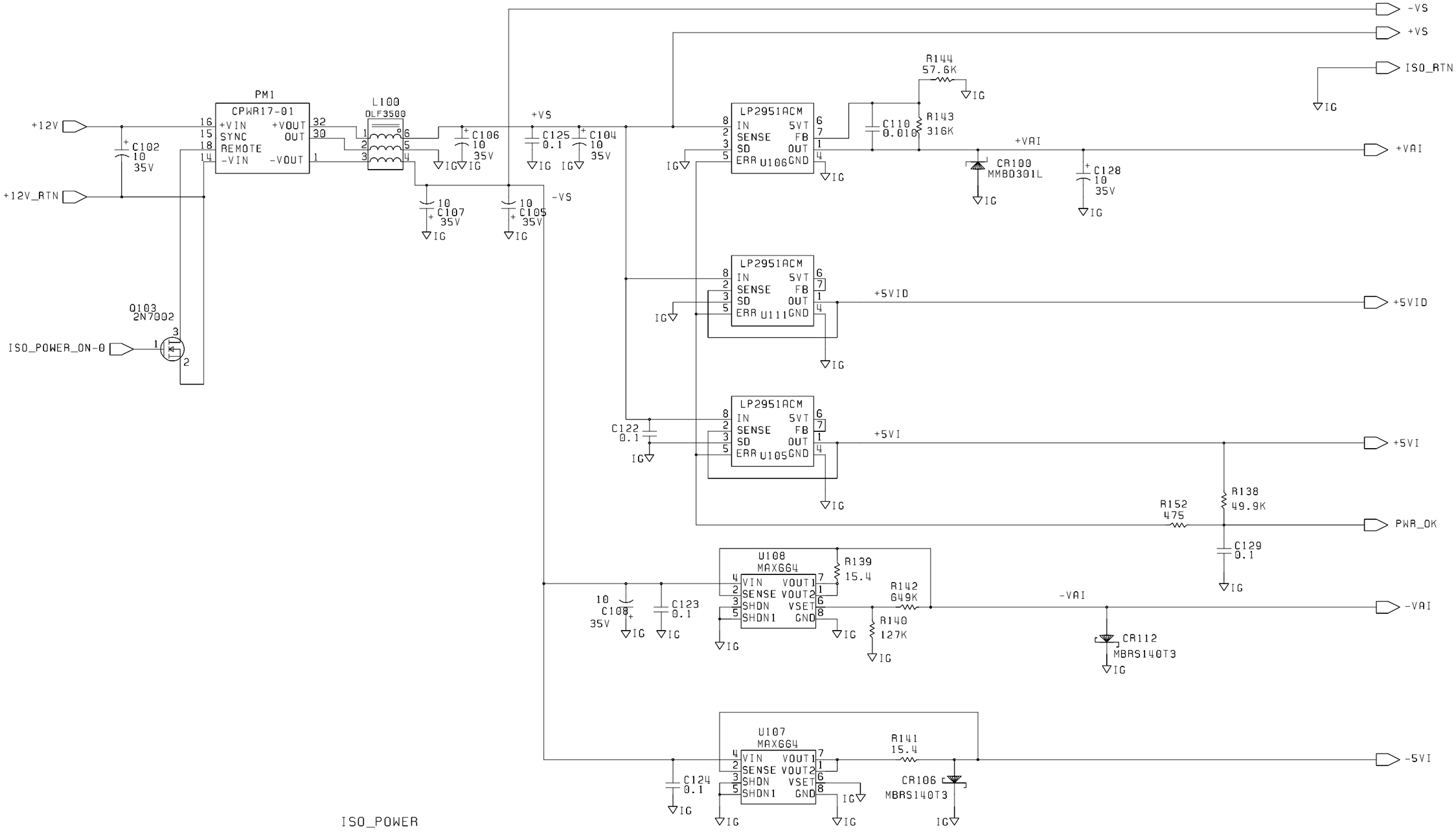
CONNECT_CONTACT
FB102
R132
1.00K
CR109
MMBD914X
CR108
MMBD914X
R128
110K
CONNECTED-0

ECG_ANALOG_OT

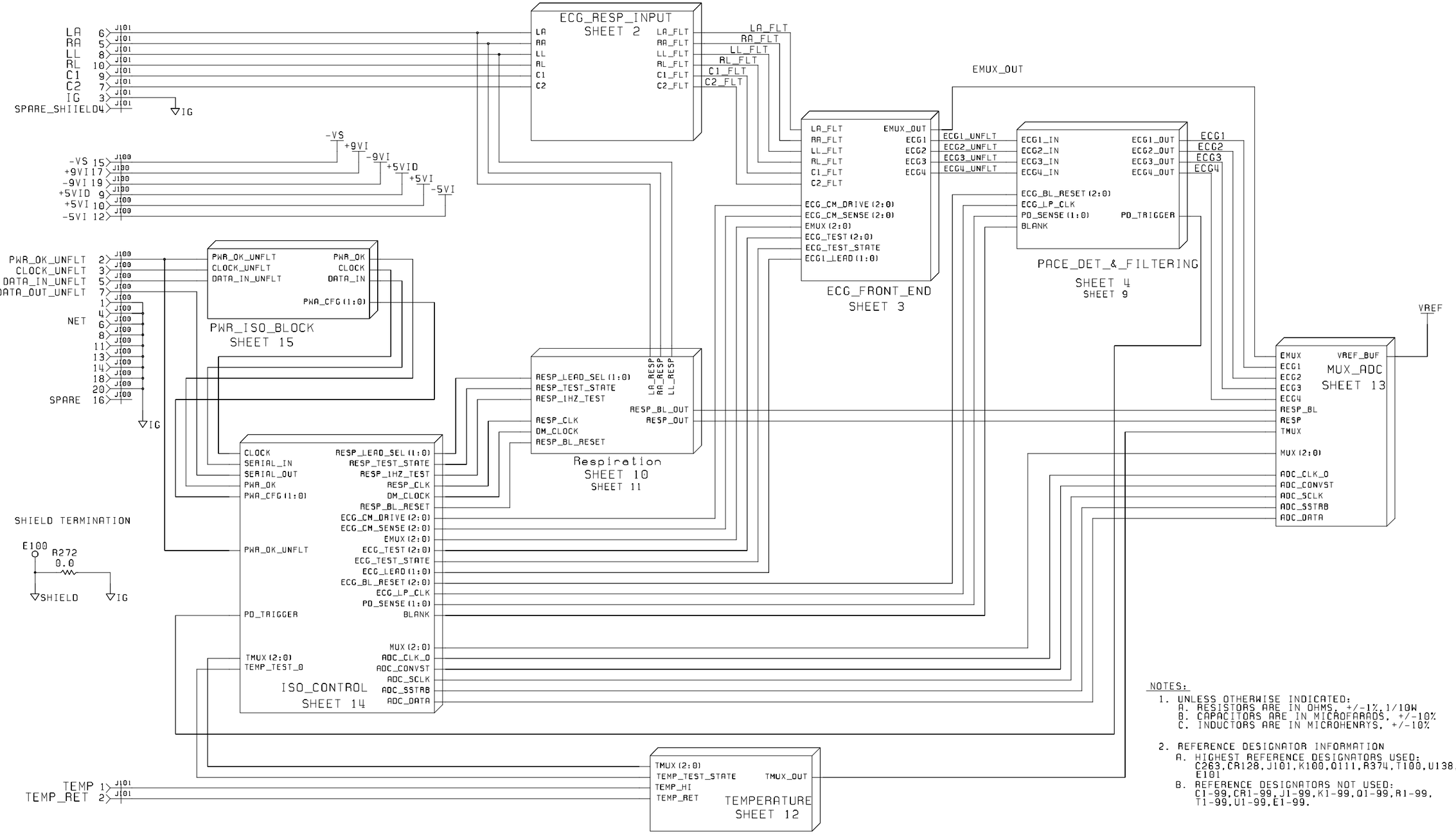
SC315-546 A
ECG Digital PWA Schematic (7 of 9)



SC315-546 A
ECG Digital PWA Schematic (8 of 9)



SC315-546 A
ECG Digital PWA Schematic (9 of 9)

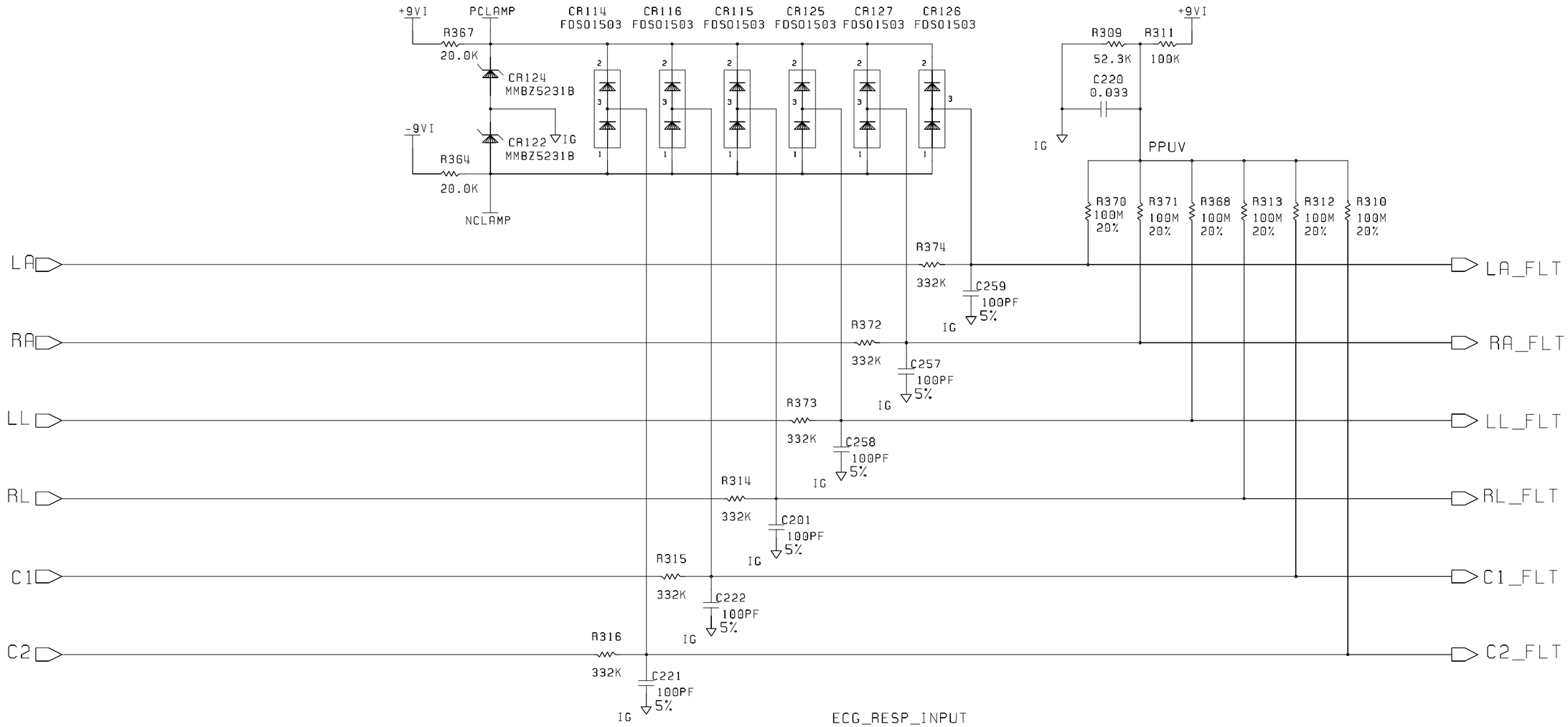


NOTES:

1. UNLESS OTHERWISE INDICATED:
   A. RESISTORS ARE IN OHMS, +/-1%, 1/10W
   B. CAPACITORS ARE IN MICROFARADS, +/-10%
   C. INDUCTORS ARE IN MICROHENRYS, +/-10%

2. REFERENCE DESIGNATOR INFORMATION
   A. HIGHEST REFERENCE DESIGNATORS USED:
      C263,CR128,J101,K100,Q111,R374,T100,U138,
      E101
   B. REFERENCE DESIGNATORS NOT USED:
      C1-99,CR1-99,J1-99,K1-99,Q1-99,R1-99,
      T1-99,U1-99,E1-99.

SC315-548 A
ECG Analog PWA Schematic (1 of 15)



SC315-548 A
ECG Analog PWA Schematic (2 of 15)

EMUX(2:0)
ECG1_LEAD(1:0)
ECG_TEST(2:0)
ECG_TEST_STATE
LA_FLT
RA_FLT
LL_FLT
C1_FLT
C2_FLT
RL_FLT
ECG_CM_DRIVE(2:0)
ECG_CM_SENSE(2:0)
EMUX_OUT
ECG1
(I, II, III)
ECG2
(II)
ECG3
(CHEST 1)
ECG4
(CHEST 2)
U132 MAX328C
U135 MAX333A
U138 TL034A
U122 TL034A
U136 TL034A
U128 DG509A
U127 DG508A
U137 MAX328C
U119 AD621
U126 AD621
U133 AD621
U134 AD621
CR120 MMBZ5222B
CR121 HSMS2804
CR123 MMBZ5222B
LA_BUF
RA_BUF
LL_BUF
RL_BUF
C1_BUF
C2_BUF
EMUX_OUT_UNBUF
ECG_ATTENUATED_TEST
ECG_TEST_OUT
ECG_2MV_TEST_IN
LA_SW_OUT
RA_SW_OUT
LL_SW_OUT
CMDRIVE_ILIM
CMDRIVE_INT
CM_FLTR_OUT
CMD_SENSE_OUT
CMD_STAGE2_NEG_INPUT
CMS_3LEAD
CM_POSTEST
CM_ZERO_TEST
CM_NEG_TEST
CMS_6LEAD
CMS_7LEAD_C1
CMS_7LEAD_C2
CMS_8LEAD
CT
VREF
IG
ECG1_NEG
ECG1_POS
ECG FRONT END

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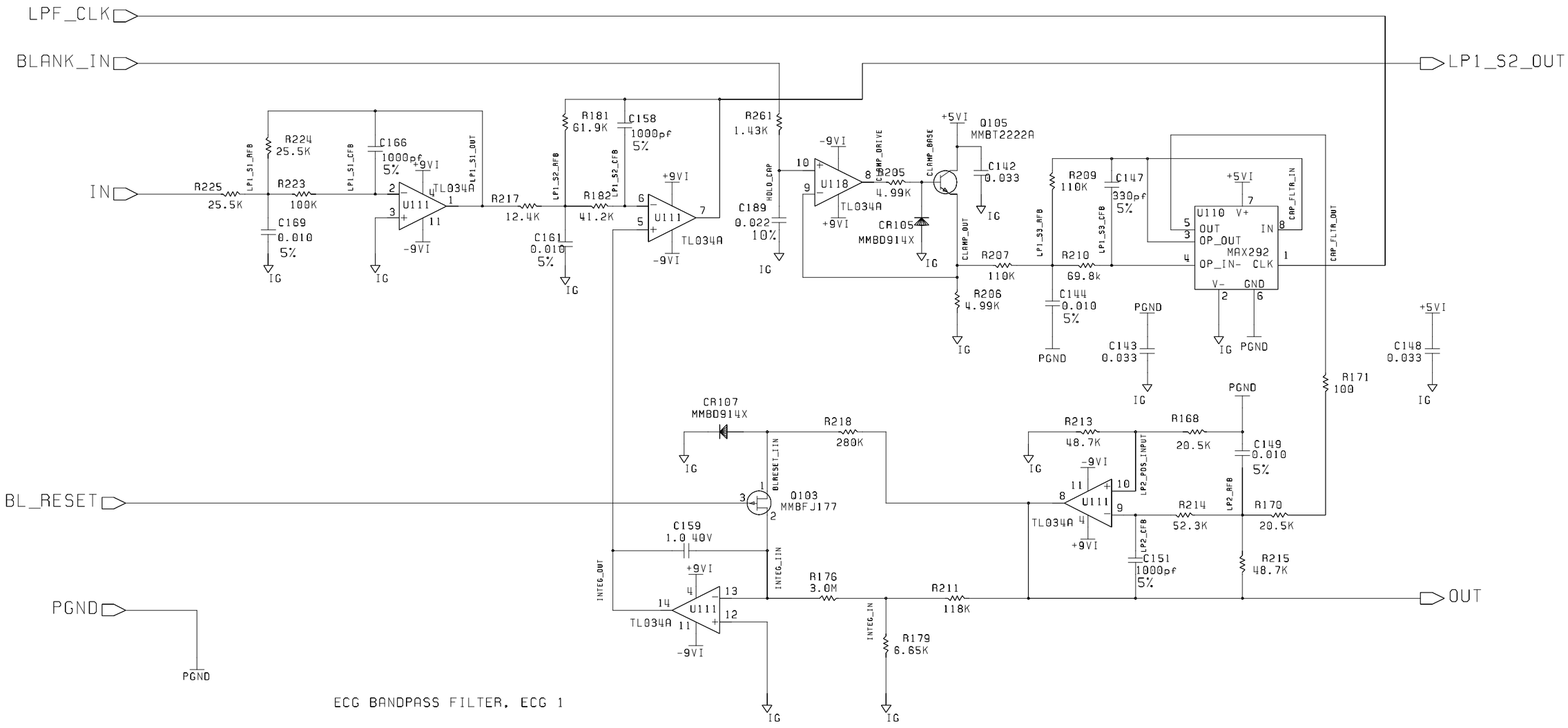
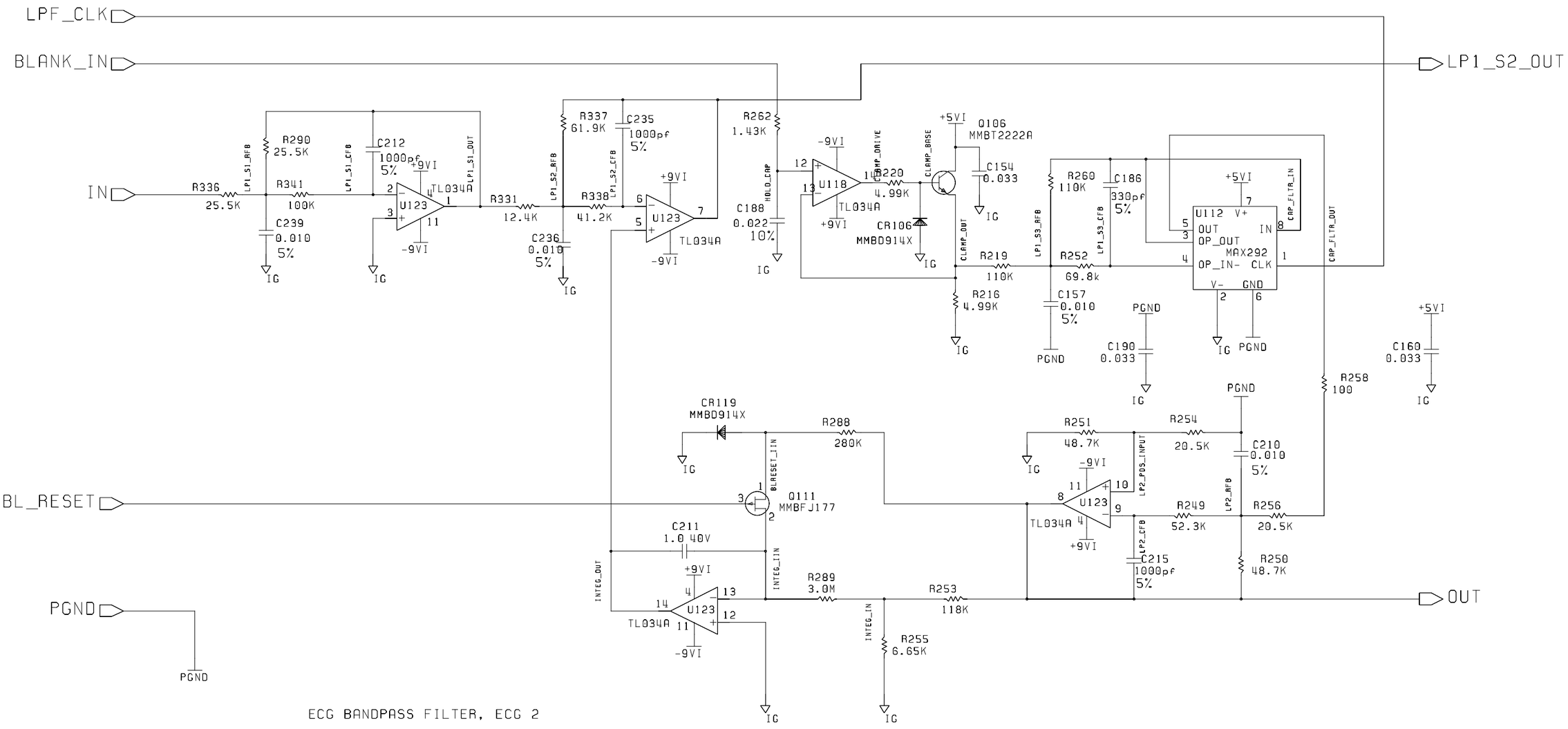
ECG Analog PWA Schematic (3 of 15)

PGND
+5VI
R334
110K
-9VI
PGND_TAP
4 TLE2062A
U131
C237
0.033
IG
R335
110K
TLE2062A
-9VI
PGND_REF
5
U131
7
R340
499
PGND_DRIVE
C246
10
IG
6
C241
0.047
R342
10.0K
PGND_FEEDBACK
R343
100K
+9VI
ECG_LP_CLK
ECG_BL_RESET(2:0)
BLANK
ECG1_IN
ECG2_IN
ECG3_IN
ECG4_IN
+5VI
R185
49.9K
IN
LPF_CLK
OUT
ECG_BANDPASS
ECG_BPF1
SHEET 5
BLANK_IN
LP1_S2_OUT
BL_RESET
PGND
ECG1_OUT
+9VI
+5VI
C187
0.033
C155
0.033
C224
0.033
C242
0.033
C233
0.033
C162
0.033
C153
0.033
C213
0.033
IG
-9VI
ECG2_OUT
ECG1_POSTBLANK
ECG2_POSTBLANK
+5VI
+9VI
U124
DG444
12
13
2
+5V
V+
3
ECG1_PREBLANK
1
15
14
ECG2_PREBLANK
16
10
11
ECG3_PREBLANK
9
7
6
ECG4_PREBLANK
8
V-
GND
4
5
-9VI
IG
ECG3_POSTBLANK
ECG4_POSTBLANK
R326
49.9K
ECG_BPF3
SHEET 7
ECG3_OUT
C185
0.033
C156
0.033
C238
0.033
C207
0.033
C132
0.033
C163
0.033
C191
0.033
ECG_BPF4
SHEET 8
R323
49.9K
ECG4_OUT
+9VI
C214
0.033
C217
0.033
C216
0.033
C203
0.033
C240
0.033
JUMPER REPLACES U125
FOR 3-LEAD ASSEMBLIES ONLY
S0
S1
S2
S3
S4
S5
S6
S7
GND
A2
A1
A0
EN
V-
V+
D
DG508A
U125
R257
10.0K
R344
0.0
PD_SENSE(1:0)
PACE_DET_AND-FILTERING
PD_TRIGGER
PACER DETECTOR
SHEET 9

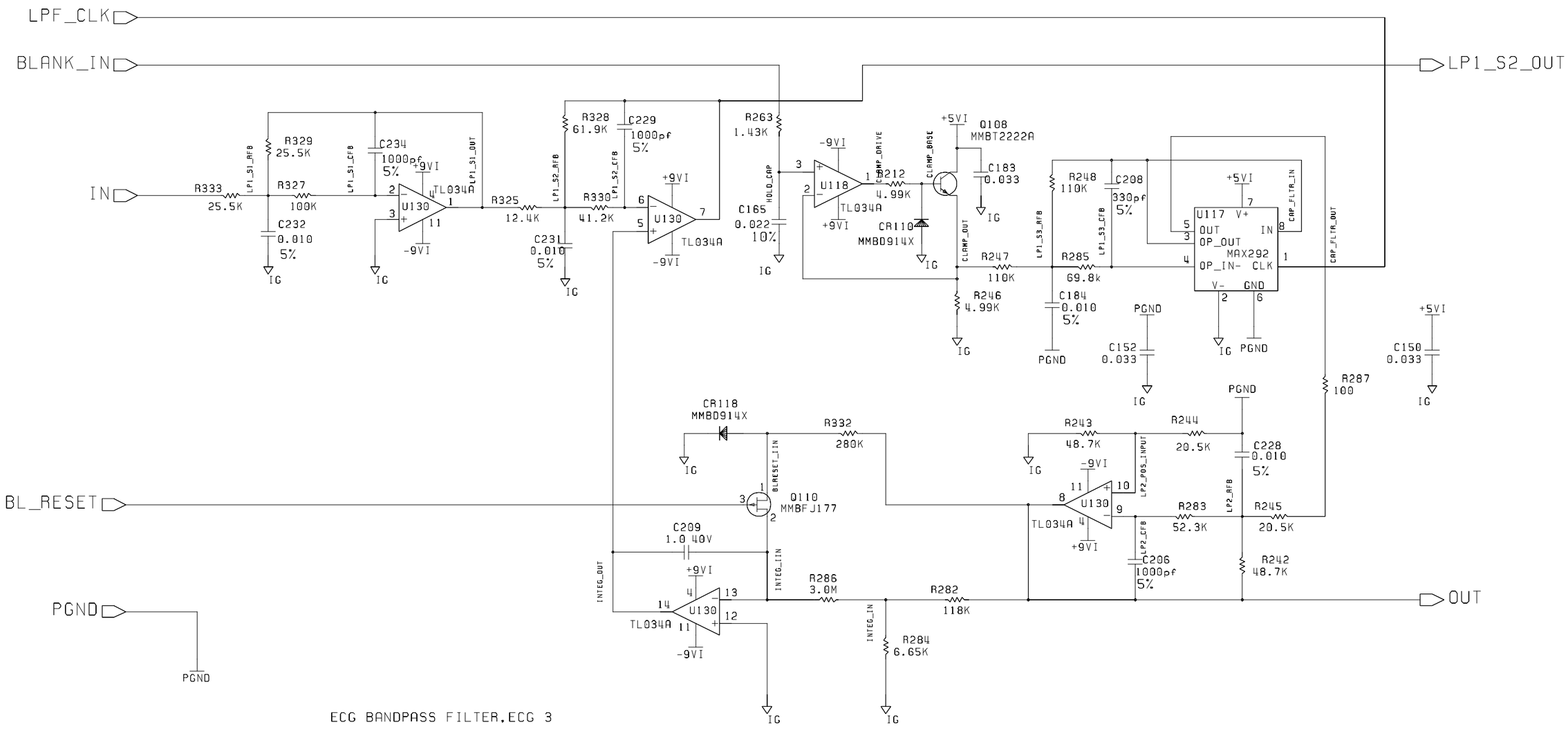
SC315-548 A
ECG Analog PWA Schematic (4 of 15)



SC315-548 A
ECG Analog PWA Schematic (5 of 15)



SC315-548 A
ECG Analog PWA Schematic (6 of 15)



ECG BANDPASS FILTER.ECG 3

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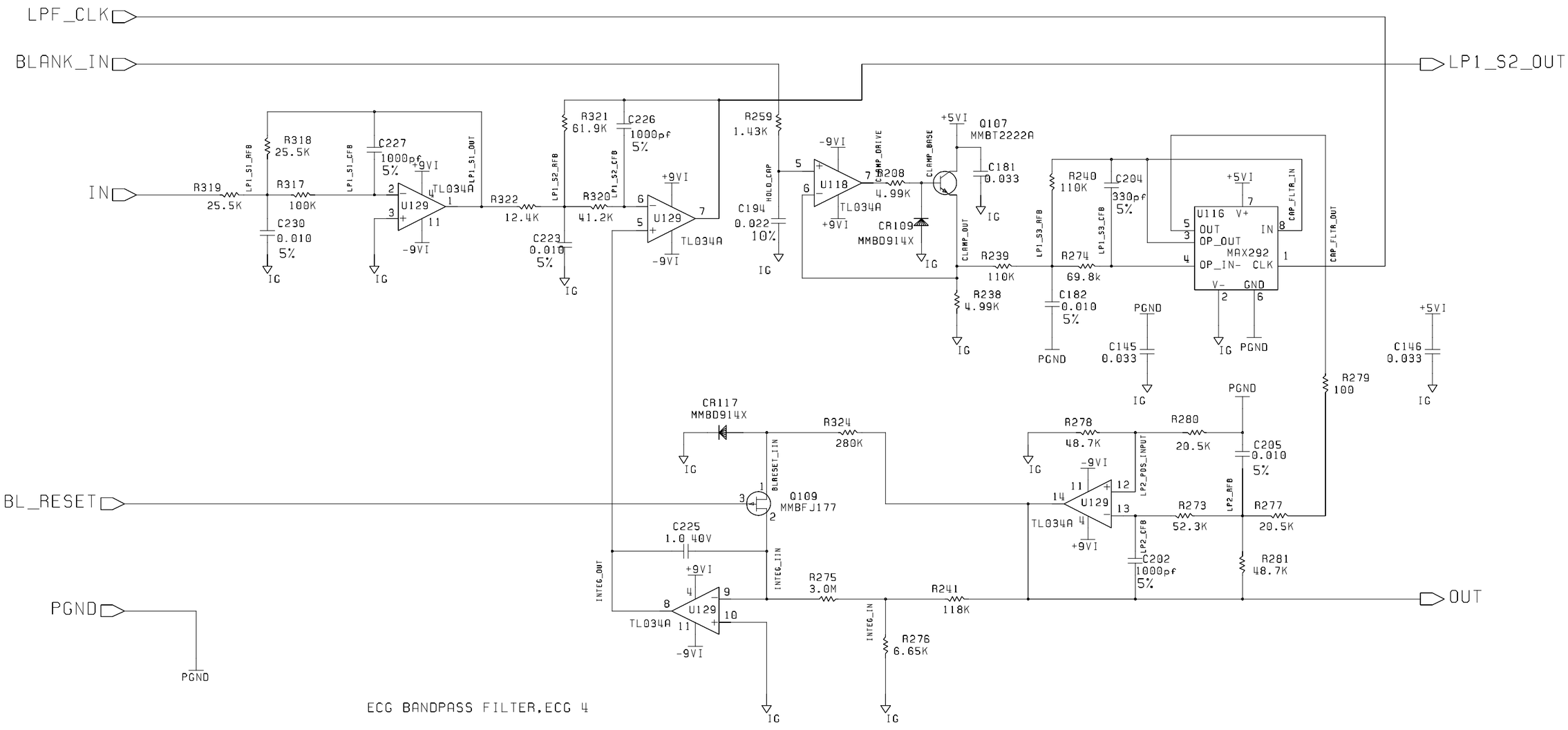
ECG Analog PWA Schematic (7 of 15)



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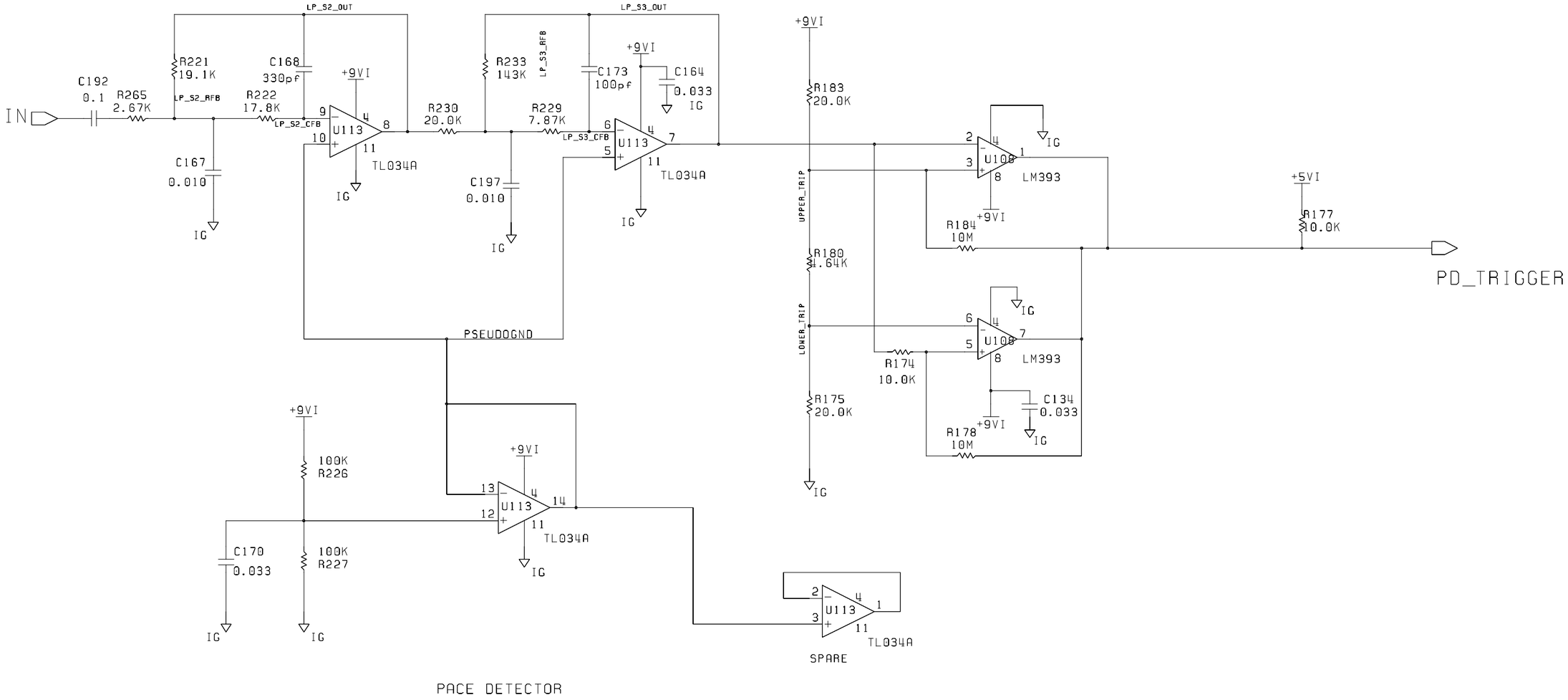
ECG Analog PWA Schematic (8 of 15)



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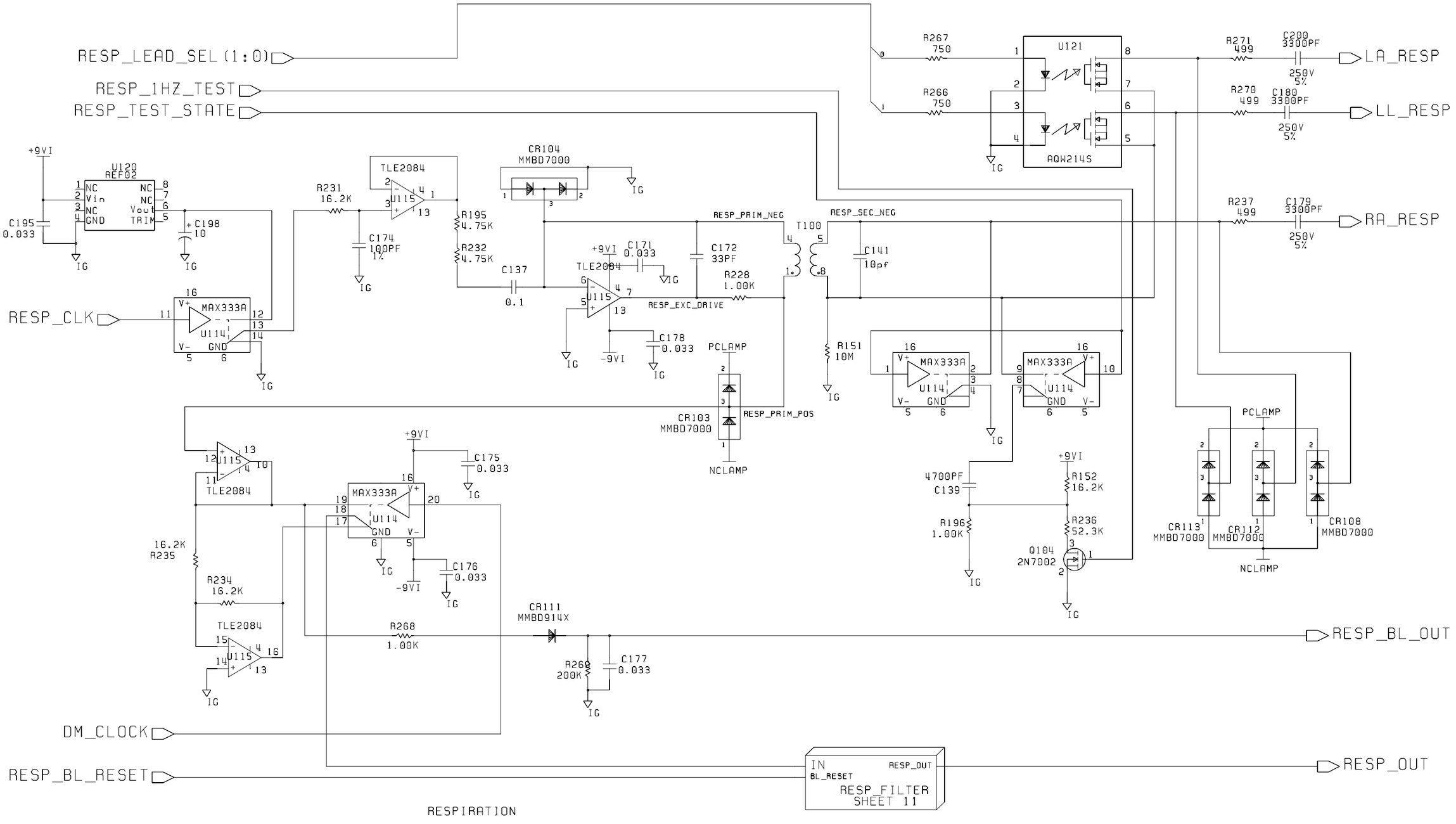
ECG Analog PWA Schematic (9 of 15)



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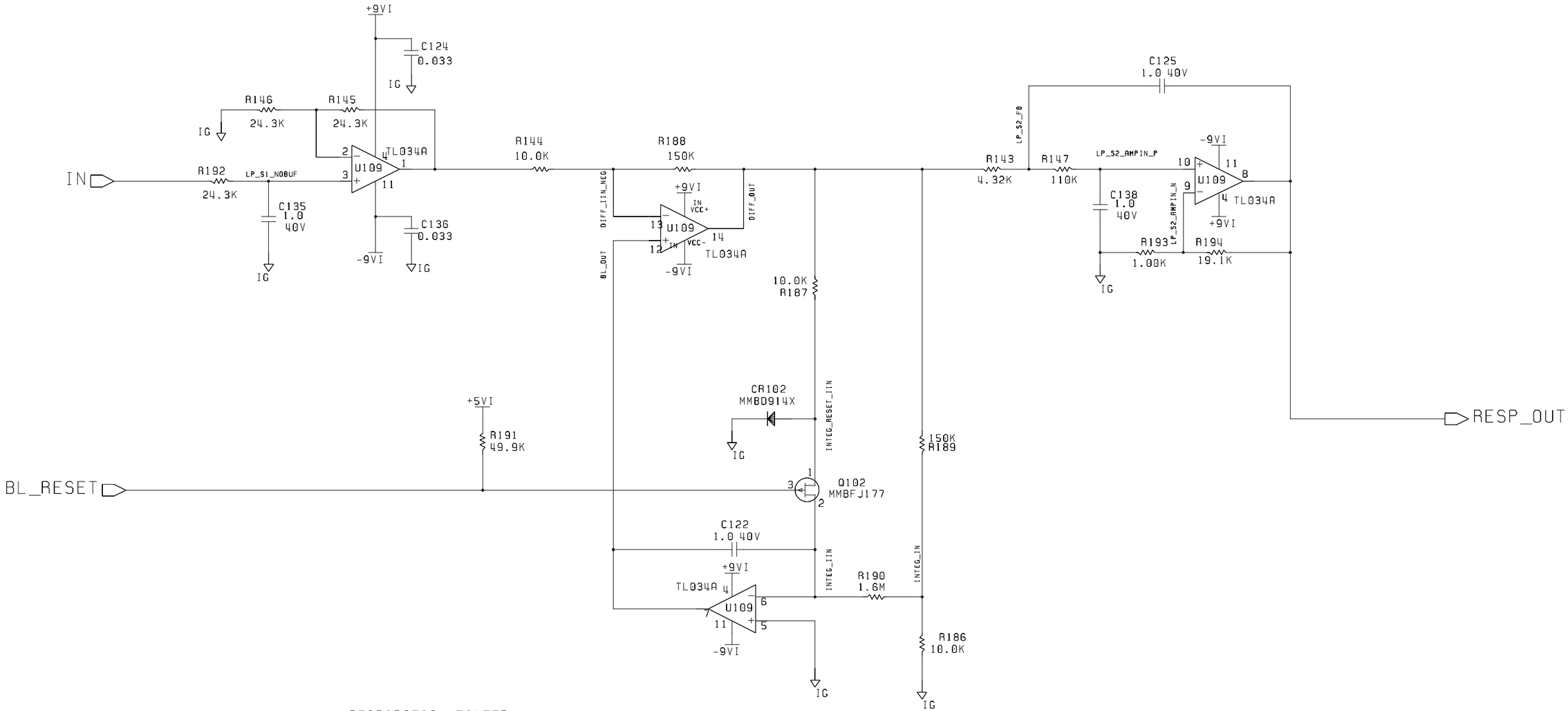
ECG Analog PWA Schematic (10 of 15)



RESPIRATION FILTER

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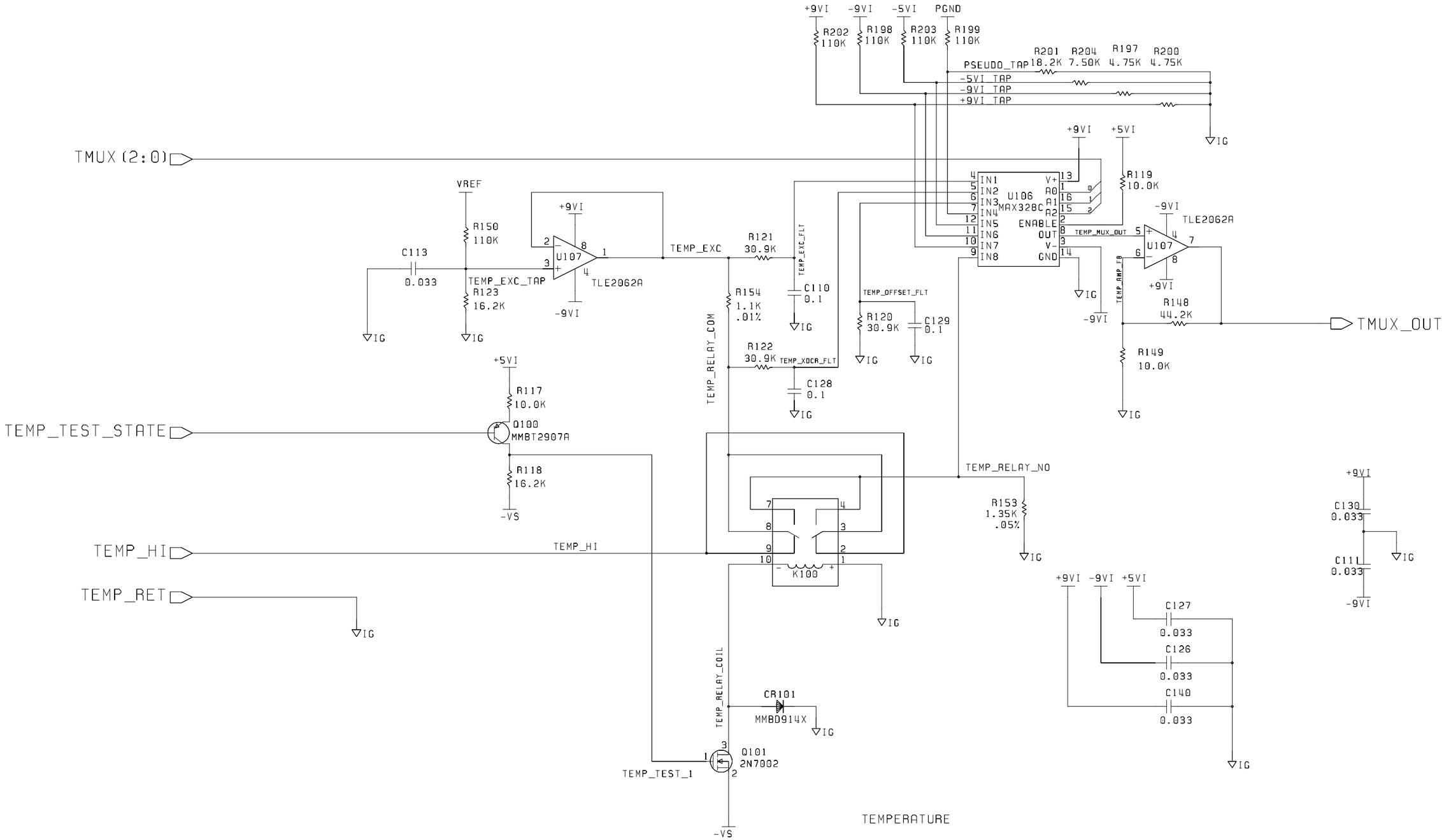
ECG Analog PWA Schematic (11 of 15)



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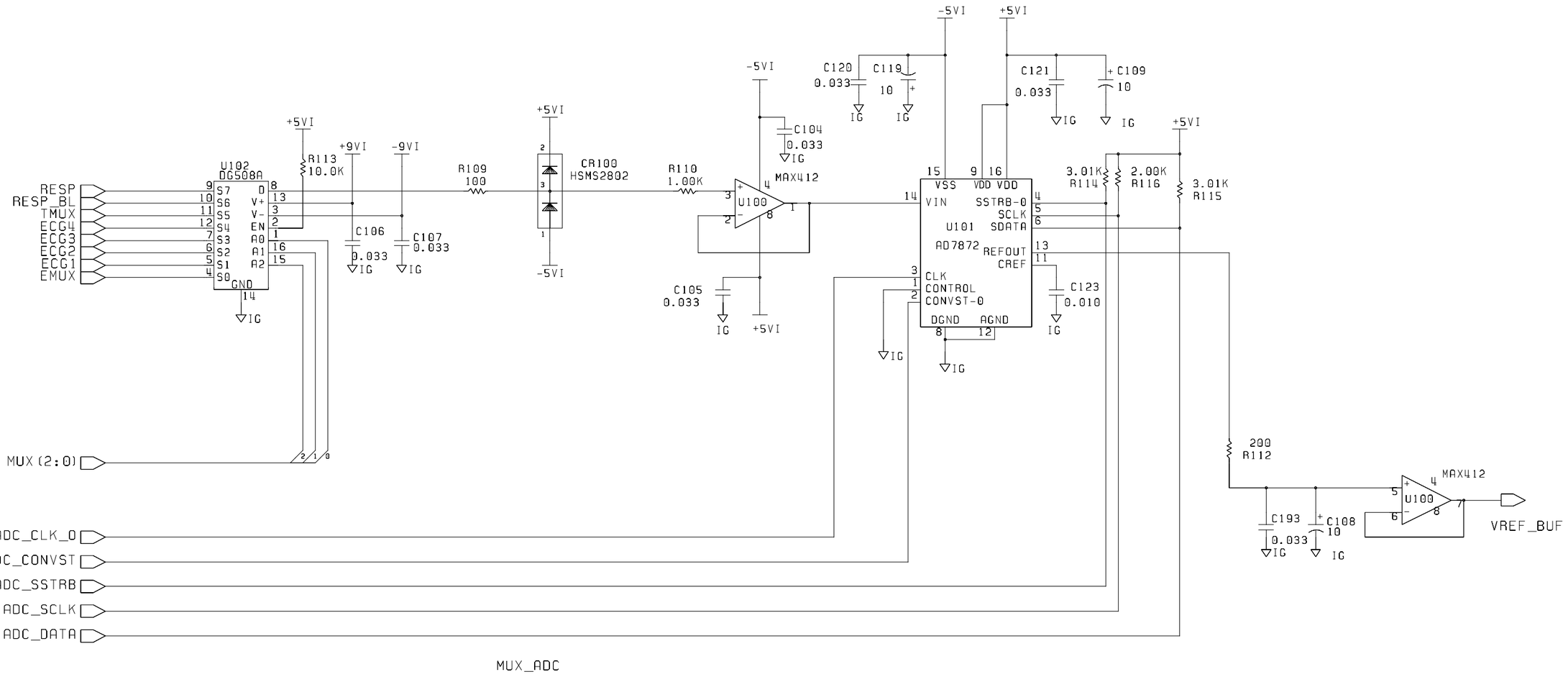
ECG Analog PWA Schematic (12 of 15)



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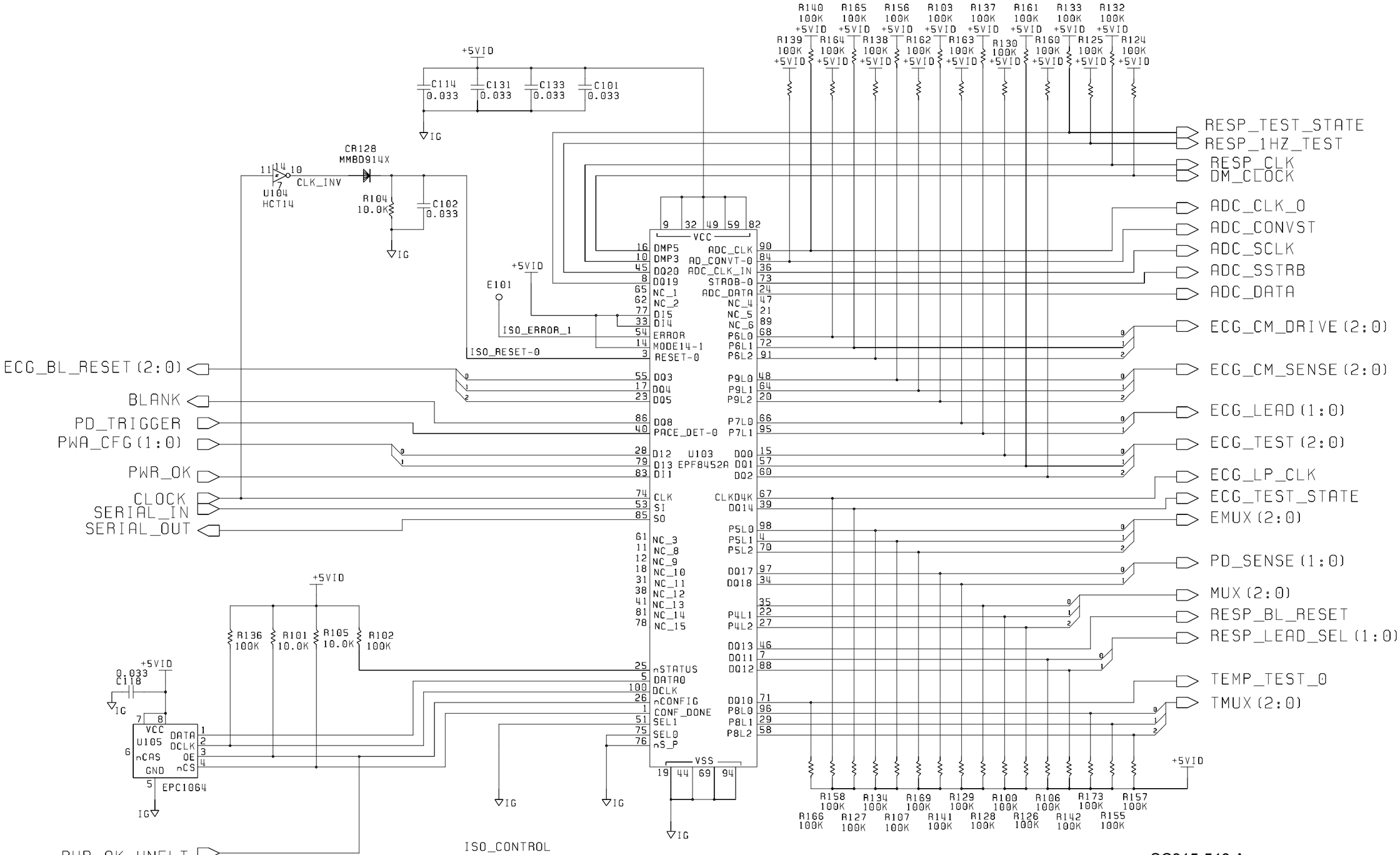
ECG Analog PWA Schematic (13 of 15)



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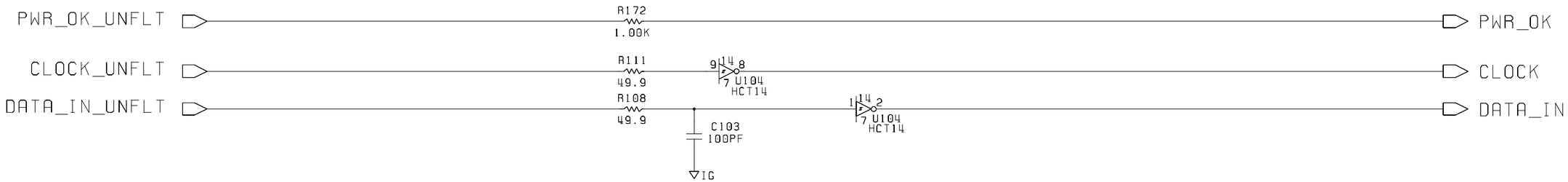
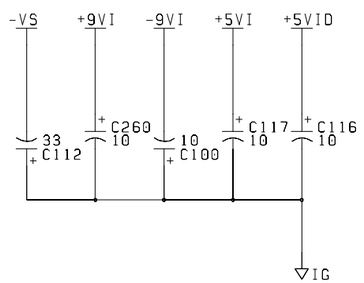
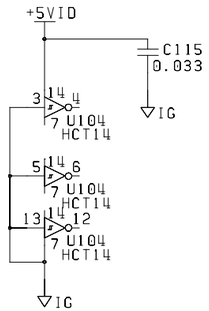
ECG Analog PWA Schematic (14 of 15)



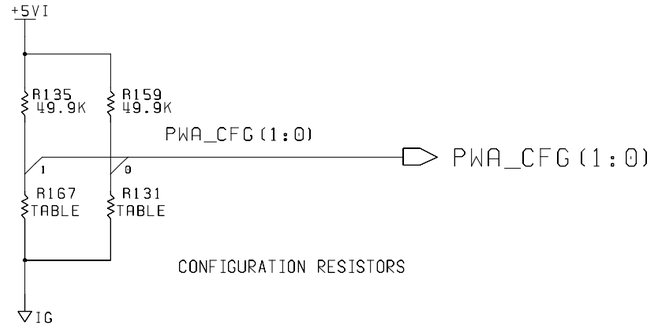




PWR & SIO BLOCK

PWA CONFIGURATION RESISTOR TABLE

ASSEMBLY	R167	R131
PL315-548	OPEN	OPEN
PL315-547	OPEN	JUMPER
	JUMPER	OPEN
	JUMPER	JUMPER



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ECG Analog PWA Schematic (15 of 15)