The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

A simplified three pin version, the LT1431Z/IZ, is available for applications as an adjustable reference and is pin compatible with the TL431.
LT1431

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>LT1431M</th>
<th>LT1431I</th>
<th>LT1431C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature Range</td>
<td>–55°C to 125°C</td>
<td>–40°C to 100°C</td>
<td>0°C to 100°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>–65°C to 150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ambient Temperature Range

- LT1431M: –55°C to 125°C
- LT1431I: –40°C to 85°C
- LT1431C: 0°C to 70°C

PACKAGE/ORDER INFORMATION

ORDER PART NUMBER

- LT1431MJ8
- LT1431CN8
- LT1431IN8
- LT1431CS8
- LT1431IS8

ORDER PART NUMBER

- LT1431CZ
- LT1431IZ

ELECTRICAL CHARACTERISTICS $T_A = 25°C, I_K = 10mA$, unless otherwise specified (Note 1).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1431M/I MIN</th>
<th>LT1431M/I MAX</th>
<th>LT1431C MIN</th>
<th>LT1431C MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>Reference Voltage</td>
<td>$V_{KA} = 5V, I_K = 2mA$, (Note 2)</td>
<td>2.490</td>
<td>2.510</td>
<td>2.490</td>
<td>2.510</td>
<td>V</td>
</tr>
<tr>
<td>$ΔV_{REF/ΔT}$</td>
<td>Reference Drift</td>
<td>$V_{KA} = 5V, I_K = 2mA$</td>
<td>50</td>
<td></td>
<td>30</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>$ΔV_{REF/ΔV_{KA}}$</td>
<td>Voltage Ratio, Reference to Cathode (Open-Loop Gain)</td>
<td>$I_K = 2mA, V_{KA} = 3V to 36V$</td>
<td>0.2</td>
<td>0.5</td>
<td>0.2</td>
<td>0.5</td>
<td>mV/V</td>
</tr>
<tr>
<td>$I_{REF}$</td>
<td>Reference Input Current</td>
<td>$V_{KA} = 5V, T_A = 25°C$</td>
<td>0.2</td>
<td>1.0</td>
<td>0.2</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>$ΔI_{REF}$</td>
<td>Reference Input Current</td>
<td>$V_{KA} = 5V, T_A = 25°C$</td>
<td>1.5</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{MIN}$</td>
<td>Minimum Operating Current</td>
<td>$V_{KA} = V_{REF} to 36V$</td>
<td>0.6</td>
<td>1.0</td>
<td>0.6</td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>Off-State Cathode Current</td>
<td>$V_{KA} = 36V, V_{REF} = 0V$</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Off-State Collector Leakage Current</td>
<td>$V_{COLL} = 36V, V^{*} = 5V, V_{REF} = 2.4V$</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{ZKA}$</td>
<td>Dynamic Impedance</td>
<td>$V_{KA} = V_{REF}, I_K = 1mA to 100mA, f ≤ 1kHz$</td>
<td>0.2</td>
<td></td>
<td>0.2</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$I_{ILIM}$</td>
<td>Collector Current Limit</td>
<td>$V_{KA} = V_{REF} + 50mV$</td>
<td>80</td>
<td></td>
<td>100</td>
<td>260</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Off-State Collector Leakage Current</td>
<td>$V_{COLL} = 36V, V^{*} = 5V, V_{REF} = 2.4V$</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

The $*$ denotes specifications which apply over the operating temperature range.

Note 1: $V_{KA}$ is the cathode voltage of the LT1431CZ/IZ and corresponds to $V^{*}$ of the LT1431C8N/M8. $I_{OFF}$ is the cathode current of the LT1431CZ/IZ and corresponds to $I(V^{*}) + I_{COLLECTOR}$ of the LT1431C8N/M8/IN8.

Note 2: The LT1431 has bias current cancellation which is effective only for $V_{KA} ≥ 3V$. A slight ($≈ 2mV$) shift in reference voltage occurs when $V_{KA}$ drops below 3V. For this reason, these tests are not performed at $V_{KA} = V_{REF}$. 

SYMBOL | PARAMETER | CONDITIONS | LT1431MZ | LT1431IZ | LT1431IZ | LT1431IZ | UNITS |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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<th></th>
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<td>2.500</td>
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<td>$ΔV_{REF/ΔT}$</td>
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<td>$V_{KA} = 5V, I_K = 2mA$</td>
<td>50</td>
<td></td>
<td>30</td>
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<td></td>
</tr>
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<td>0.5</td>
<td>0.2</td>
<td>0.5</td>
<td>mV/V</td>
</tr>
<tr>
<td>$I_{REF}$</td>
<td>Reference Input Current</td>
<td>$V_{KA} = 5V, T_A = 25°C$</td>
<td>0.2</td>
<td>1.0</td>
<td>0.2</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>$ΔI_{REF}$</td>
<td>Reference Input Current</td>
<td>$V_{KA} = 5V, T_A = 25°C$</td>
<td>1.5</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{MIN}$</td>
<td>Minimum Operating Current</td>
<td>$V_{KA} = V_{REF} to 36V$</td>
<td>0.6</td>
<td>1.0</td>
<td>0.6</td>
<td>1.0</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>Off-State Cathode Current</td>
<td>$V_{KA} = 36V, V_{REF} = 0V$</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{LEAK}$</td>
<td>Off-State Collector Leakage Current</td>
<td>$V_{COLL} = 36V, V^{*} = 5V, V_{REF} = 2.4V$</td>
<td>1</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$I_{ZKA}$</td>
<td>Dynamic Impedance</td>
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<td></td>
<td>0.2</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$I_{ILIM}$</td>
<td>Collector Current Limit</td>
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<td>80</td>
<td></td>
<td>100</td>
<td>260</td>
<td>mA</td>
</tr>
</tbody>
</table>
**TYPICAL PERFORMANCE CHARACTERISTICS**

**2.5V Reference I_k vs V_KA**

**V_{REF} and I_{REF} vs V^+**

**V_{REF} and I_{REF} vs Temperature**

**I_{LIMIT} vs Temperature with External Resistor**

**COLLECTOR V_{SAT} vs Temperature vs Current**

**Propagation Delay vs Overdrive**
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency

Transconductance and Phase vs Frequency (REF to COLL)

Transconductance and Phase vs Frequency (Ref to Comp)

Dynamic Impedance vs Frequency

V_{COMP} vs Temperature vs I_{COLL}

I_{COMP} vs V_{COMP} vs V_{REF}

Noise vs Frequency

0.1Hz to 10Hz Noise
PIN FUNCTIONS

COLL (Pin 1): Open collector of the output transistor. The maximum pin voltage is 26V. The saturation voltage at 100mA is approximately 1V.

COMP (Pin 2): Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

V+ (Pin 3): Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to VREF (2.5V). The quiescent current is typically 0.6mA.

RTOP (Pin 4): Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

GND-S (Pin 5): Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

GND-F (Pin 6): Emitter of the output transistor and substrate connection for the die.

RMID (Pin 7): Middle of the on-chip resistive divider string between RTOP and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

REF (Pin 8): Control pin of the shunt regulator with a 2.5V threshold. If V+ > 3V, input bias current cancellation reduces IB to 0.2µA typical.

COMP, RTOP, RMID, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are RTOP below RMID in voltage and any pin below GND-F in voltage (except for GND-S).

The following pin definitions apply to the Z package.

CATHODE (Pin 1): Corresponds to COLL and V+ tied together.

ANODE (Pin 2): Corresponds to GND-S and GND-F tied together.

REF (Pin 3): Corresponds to REF.

BLOCK DIAGRAM

![Block Diagram of LT1431](image-url)
Frequency Compensation

As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01µF and 18µF causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency response of the LT1431 with dominant pole or pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.
TYPICAL APPLICATIONS

PNP Low Dropout 5V Regulator*

- 1kΩ
- 150Ω
- 0.015µF

MEASURED DROPOUT VOLTAGE
- 420mV AT 4A
- 190mV AT 2A
- 95mV AT 1A
- 60mV AT 0.5A

*NO SHORT-CIRCUIT PROTECTION
**MAY BE INCREASED AT LOWER WATTAGE FOR LOWER OUTPUT CURRENTS

FET Low Dropout 5V Regulator with Current Limit

Measured Dropout Voltages

<table>
<thead>
<tr>
<th>I_LOAD</th>
<th>MTP50N05EL</th>
<th>MTM25N05L</th>
</tr>
</thead>
<tbody>
<tr>
<td>2A</td>
<td>47mV</td>
<td>145mV</td>
</tr>
<tr>
<td>1A</td>
<td>22mV</td>
<td>73mV</td>
</tr>
<tr>
<td>0.5A</td>
<td>11.5mV</td>
<td>37mV</td>
</tr>
</tbody>
</table>

*1.5" #23 SOLID COPPER WIRE
~0.002Ω → 3A LIMIT
**TYPICAL APPLICATIONS**

**12V to 5V Buck Converter with Foldback Current Limit***

![Circuit Diagram](image)

- **LT1172**
  - 56% at 2.2W out
- **LT1072**
  - 56% at 2.2W out
- **LT1071**
  - 56% at 4.4W out

---

**Isolated 5V to ±15V Flyback Converter**

![Circuit Diagram](image)

**Buck Converter Efficiency**

![Graph](image)

**Fully Loaded Output Ripple vs Filtering**

<table>
<thead>
<tr>
<th>C*</th>
<th>LT1172</th>
<th>LT1072</th>
</tr>
</thead>
<tbody>
<tr>
<td>210µF</td>
<td>30mVP-P</td>
<td>40mVP-P</td>
</tr>
<tr>
<td>100µF</td>
<td>6mVP-P</td>
<td>8mVP-P</td>
</tr>
</tbody>
</table>

---

*CONTACT LTC FOR HIGH EFFICIENCY SWITCHING REGULATORS*
**High Efficiency Buck Converter E = 85% to 89%**

**NOTES: UNLESS OTHERWISE SPECIFIED**
1. ALL RESISTANCES ARE IN Ω, 0.25W, 5%
2. ALL CAPACITANCES ARE IN µF, 50V, 10%
3. SHUTDOWN LOGIC STATE MUST BE DEFINED BY A LOGIC GATE OR BY TYPING TO GND

---

**BOLD LINE INDICATES HIGH CURRENT PATHS**
- 1% FILM RESISTORS
- C1 = NICHICON-UP11V221MPH
- C6 = NICHICON-UP11C471MPH6
- D1, D2 = PHILIPS-BAT85
- D3 = MOTORALA-MBR330
- L1 = COILTRONICS CTX50-3-MP
- C3, C4, C5 = WIMA-MKS-2

**“HIGH” FOR OVER VOLTAGE OR UNDER VOLTAGE**

**V = (R – 5)(0.5mA)**

**SETS HYSTERESIS**

---

**TYPICAL APPLICATION**

*5V Power Supply Monitor with ±500mV Window and 50mV Hysteresis*
**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

### J8 Package
8-Lead Ceramic DIP

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Lower Limit</th>
<th>Upper Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
<td>0.300 – 0.320</td>
<td>0.325 +0.025</td>
</tr>
<tr>
<td>Height</td>
<td>0.009 – 0.015</td>
<td>0.025 –0.015</td>
</tr>
<tr>
<td>Termination Angle</td>
<td>0° – 15°</td>
<td>0.025 (0.635)</td>
</tr>
</tbody>
</table>

### N8 Package
8-Lead Plastic DIP

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Lower Limit</th>
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<tr>
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<td>0° – 15°</td>
<td>0.025 (0.635)</td>
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</tbody>
</table>

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of circuits as described herein will not infringe on existing patent rights.
PACKAGE DESCRIPTION  Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic SOIC

Z Package
3-Lead TO-92